Memorandum

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From: J. Effland

Date: 2000-11-07 (Revised 2000-11-09 concerning discussion of Grammer's circuit)

Subject: Stability Analysis of SIS Mixer Bias Supply

1. Summary

The SIS mixer bias supplies, designed by A. R. Kerr[1], normally employ a voltage feedback loop to maintain a constant bias voltage at the mixer. Long after the design of the bias supply, isolation resistors[2] were introduced in the bias tees to minimize static discharge damage. However, mixer bias instability has been observed in the SIS lab when using the bias tees with these isolation resistors.

A stability analysis of the bias supply is presented in this memo, along with a proposed solution in the form of pole-zero compensation of the loop. The phase margin has been increased from a few degrees to a minimum of about 37 degrees with the compensation network. Measured results of the compensation network are also included here and qualitatively agree with the analysis.

2. Bias Supply Circuit

The circuit analyzed is shown in Figure 1 and the details are summarized in Table 1. The op amps used for the simulation are mostly the updated models selected by Wes Grammer in his design[3]. That design uses updated components of the A.R. Kerr design, PC cards installed in pods on the Dewar wall, and filter capacitors moved to the high signal level side of the circuit. Hence, the Grammer design is not susceptible to the instabilities documented in this memo.

The vendor specifies the feed-through filters as having 1 μF minimum capacitance, but the value quoted in Table 1 was found to most closely match the specified rejection levels.

[1] "SIS Bias Supply, Type II," schematic from A.R. Kerr dated 1982-08-27.
[2] "The NRAO Type 2B 1-2 GHz SIS Bias-T," NRAO Electronics Division Technical Note # 173, A. R. Kerr and D. Boyd, 1996-02-15.
[3] "MMA Receiver SIS Bias Card Type IIB (6-wire)," schematic from Wes Grammer, dated 1999-04-30.

Table 1 : Circuit Details Used for Bias Supply Simulation	
Mixer:	R13 and C3
Bias tee:	R10, R11, R12
	10K isolation resistors: R20, R35, R36
Lead-lag circuit:	R9, R31, and C28
Feed-through filters (Spectrum Control 9001-100-1010):	Pi Network comprised of 0.322 μF, 0.6 ohms and 0.396 mH inductance.
Cable capacitance (Belden 8163) :	220 pF conductor to ground and 125 pF between conductors

3. Circuit Analysis

The circuit was analyzed using "Electronics Workbench" Version 5.12 from Interactive Image Technology. The 50-MΩ resistor, R22, is not in Kerr's original design, but is required for convergence of the analysis routines.

The feed-through filters used in the SIS laboratory Dewars are located in pods attached to the Dewar walls. These filters significantly influence the closed-loop performance, and hence attempts were made to model them carefully. The filter manufacturer, Spectrum Control Engineering, was unable to provide any more information, such as an equivalent circuit, than is available from the catalog. The catalog states that these filters are of the Pi type, so the circuit shown in Figure 1 was used. The performance of this circuit with 50 Ω terminations was compared to the manufacturer's specs in Figure 2. The frequency response of the model filter was designed to match the specified manufacturer's response at lower attenuation values, which are more critical for the loop analysis. No attempt was made to model parasitic elements that produce the rapid rolloff at high attenuations, since this should not significantly affect loop performance.

4. Pole-Zero Compensation Network

Several standard approaches[4] were attempted to improve the stability of the bias supply in closed loop mode. All approaches were subject to the following constraints:

1. The loop bandwidth must be sufficient to permit swept I-V measurements and to simplify manual bias adjustments.
2. The compensation network should be simple, because there may be up to eight such circuits required for each ALMA cartridge.
3. The system should be stable for all source impedances and for mixers with and without protection resistors.

Dominant pole compensation was attempted by simply increasing the capacitance of the integrating capacitor C6 from 0.01 μF to 1 μF. Although excellent stability can be achieved, the loop bandwidth is unacceptably small: only 0.5 Hz with 2K-source resistance and no isolation resistors.

Lead-lag, or pole-zero compensation produces acceptable results. This technique involves adding a zero to cancel the lowest frequency pole, then adding another pole to yield a transfer function whose gain is 0 dB at the second

[4] Millman and Halkias, "Integrated Electronics: Analog and Digital Circuits and Systems," McGraw-Hill, 1972, p 477.

pole of the uncompensated network. The zero (f_{zero}) and pole (f_{pole}) frequencies are given by the following equations, using the reference designations in Figure 1:

$$f_{zero} = \frac{1}{2\pi R_{31} C_{28}}$$

$$f_{pole} = \frac{1}{2\pi (R_9 + R_{31}) C_{28}}$$

The lowest frequency pole is found to be about 0.3 Hz from the 135° phase crossing on any of the uncompensated bode plots (*e.g.*, Figure 8). Component values shown in Figure 1 were first determined from the above equations, then empirically optimized for the embedded impedances seen by the lead-lag circuit.

The laboratory version of the bias supply includes an open-loop mode to provide for manual sweeping of the bias voltage. The compensation network described in this memo remains in the circuit and thus needlessly reduces loop bandwidth during this open-loop mode. Additional work is planned to move it out of the open-loop circuit without introducing additional circuit complexity. Open loop mode is probably not required for the ALMA production receivers.

5. Analysis Results

The closed loop bias circuit will oscillate if the phase shift of the loop decreases to 0° while the loop gain is greater than zero. The phase margin is defined as the loop phase at the frequency where the loop gain is 0 dB. Figure 3 is a summary of the phase margins achieved with and without compensation for mixers both with and without isolation resistors. The source resistance is the abscissa of the graph, since this is selectable in the laboratory version of the bias supply. Without the lead-lag compensation network, the bias supply is only marginally stable with a source resistance of 100 Ω into a mixer with isolation resistors. Figure 3 shows that the bias supply is unstable with higher source resistances, which is also supported by observations in the lab. With the compensation network, the system remains stable with a minimum phase margin of about 37° using 100-ohm source into a mixer with isolation resistors.

The 0-dB loop bandwidth, summarized in Figure 4, shows the inevitable bandwidth decrease with the compensation network. The smallest loop bandwidth is about 30 Hz, which is sufficient for automated bias curve measurements, but is too small for manually sweeping the bias in real-time. Hence, it is important to be able to remove the compensation network when open-loop mode is selected.

Bode plots for all the cases analyzed are itemized in the table below:

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6. Comparison to Measured Results

Measured data was obtained and compared to several analysis cases. The external input of the bias supply was driven by a square wave and the closed loop voltage *vs.* time was measured. Mixer voltage in the Dewar was observed with a Tektronix TDS 3032 oscilloscope across a 100 Ω resistor simulating the mixer. A HP 3310A function generator provided a square wave to the external bias input of the Type IIC mixer bias supply. The results are summarized in Table 2.

Table 2: Comparison of Measured and Simulated Data

Simulated Data	Measured Data	Compen-sation	Source resistance	Notes
Figure 15	Figure 16	None	100 Ω	The simulated data shows a faster decay of the ringing, but the qualitative comparisons seem reasonable.
Figure 17	(See Notes)	None	2 KΩ	Measured data for this case is not available because the bias supply oscillates since the analysis shows that the phase margin is only a few degrees.
Figure 18	Figure 19	Lead-Lag	100 Ω	Despite the high noise level in the measured data, qualitative agreement between simulated and measured data is good.
Figure 20	Figure 21	Lead-Lag	2 KΩ	

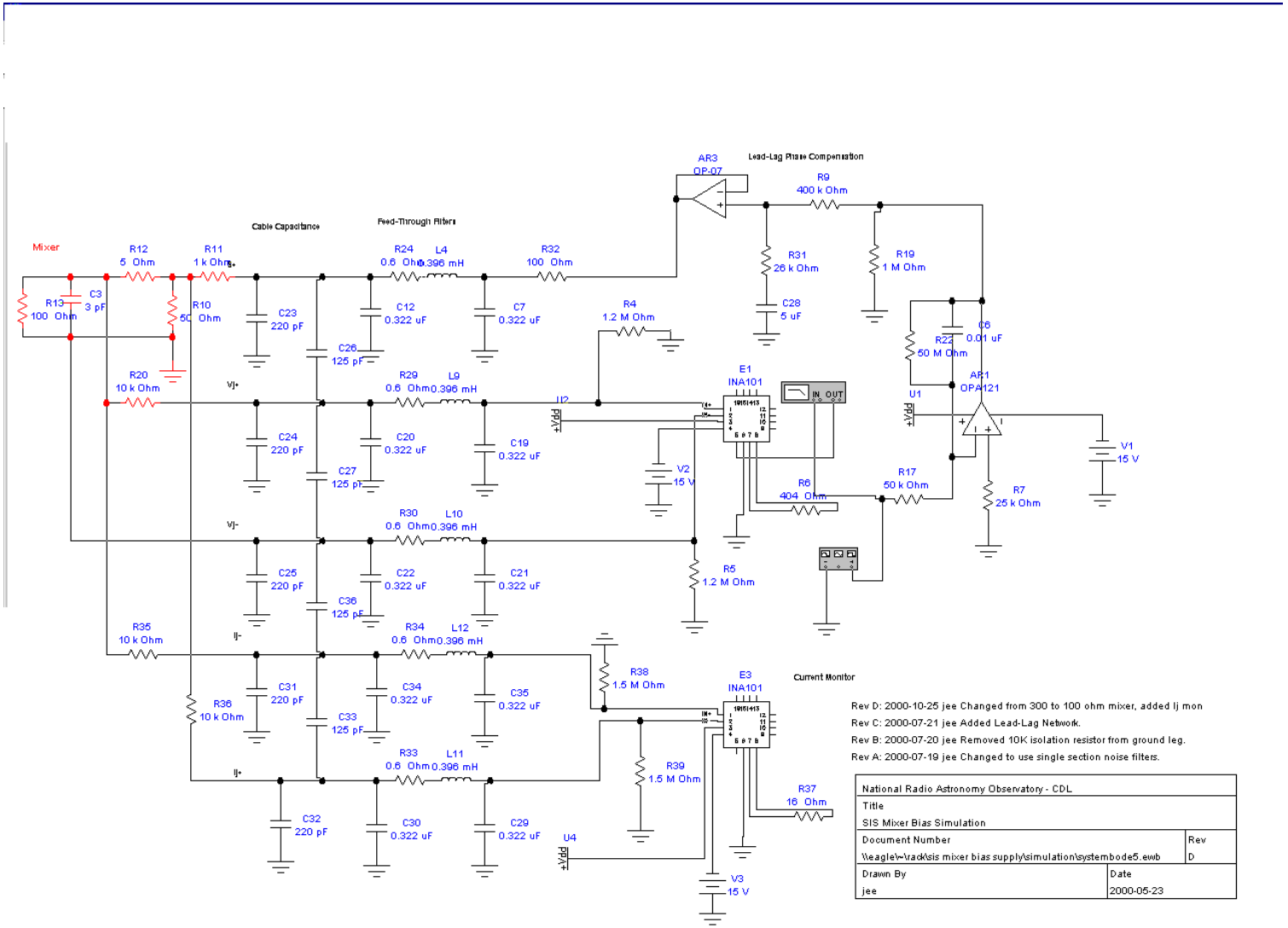

Figure 1: Bias Supply Circuit Used for Analysis

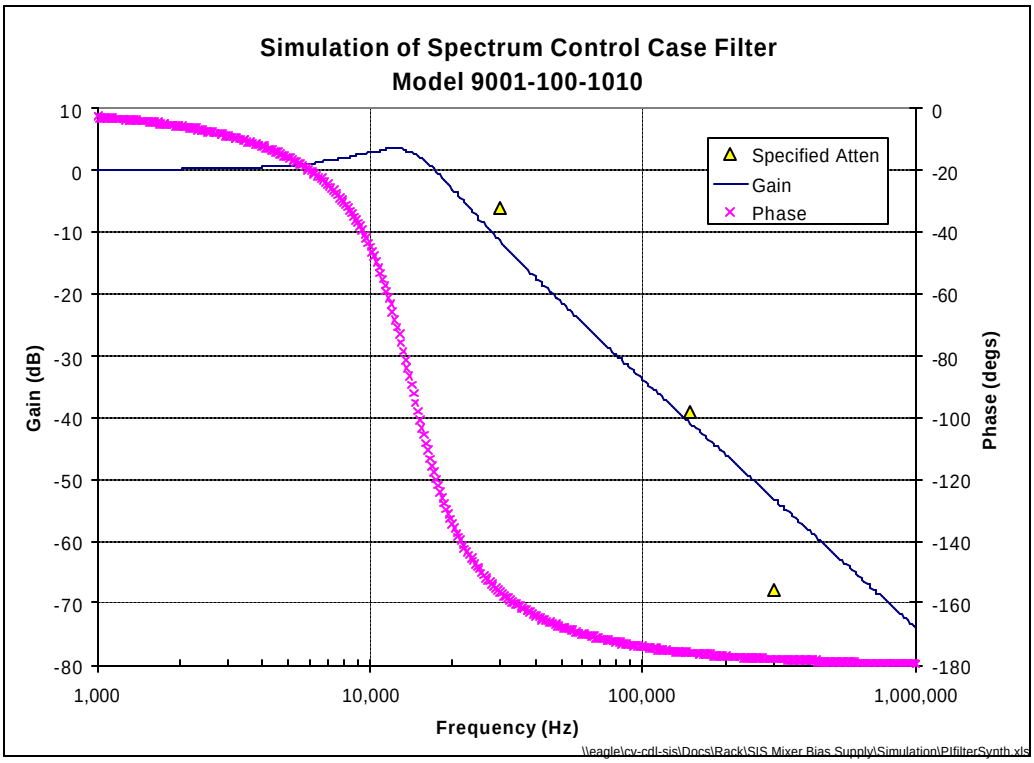

Figure 2: Analysis of Spectrum Control Feed-Through Filter

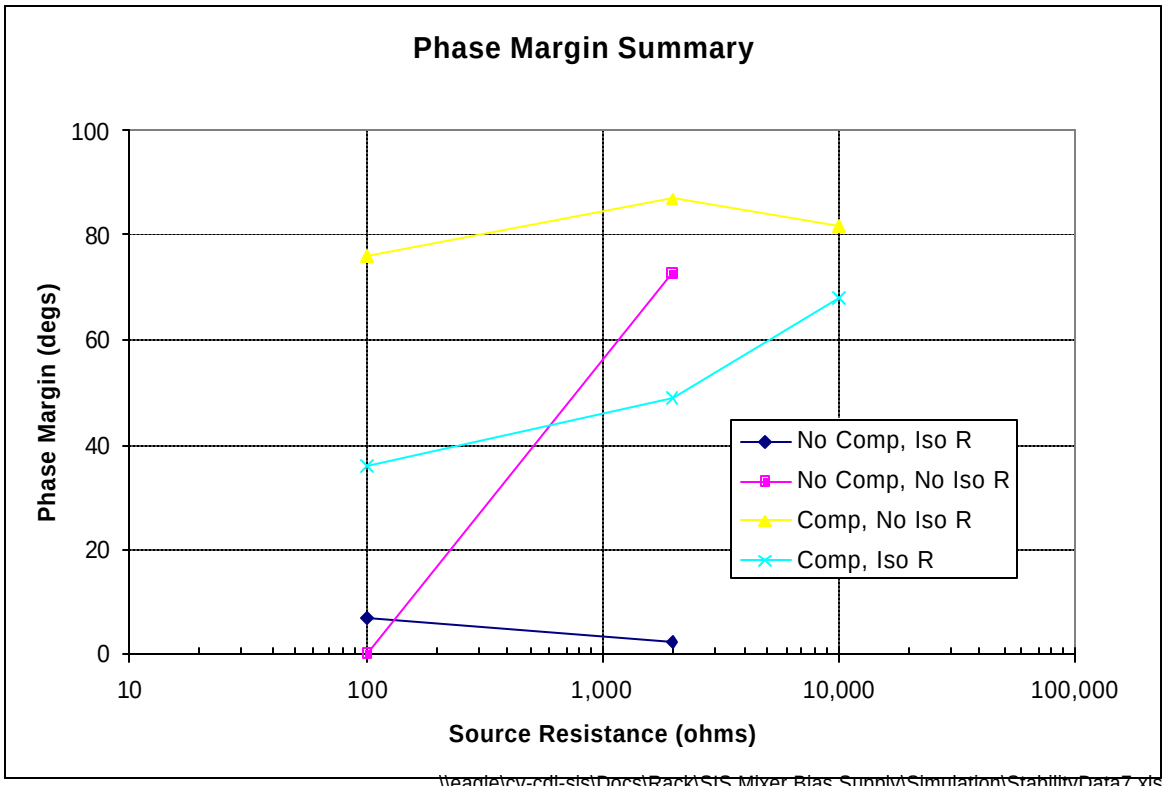

Figure 3: Phase Margin Summary

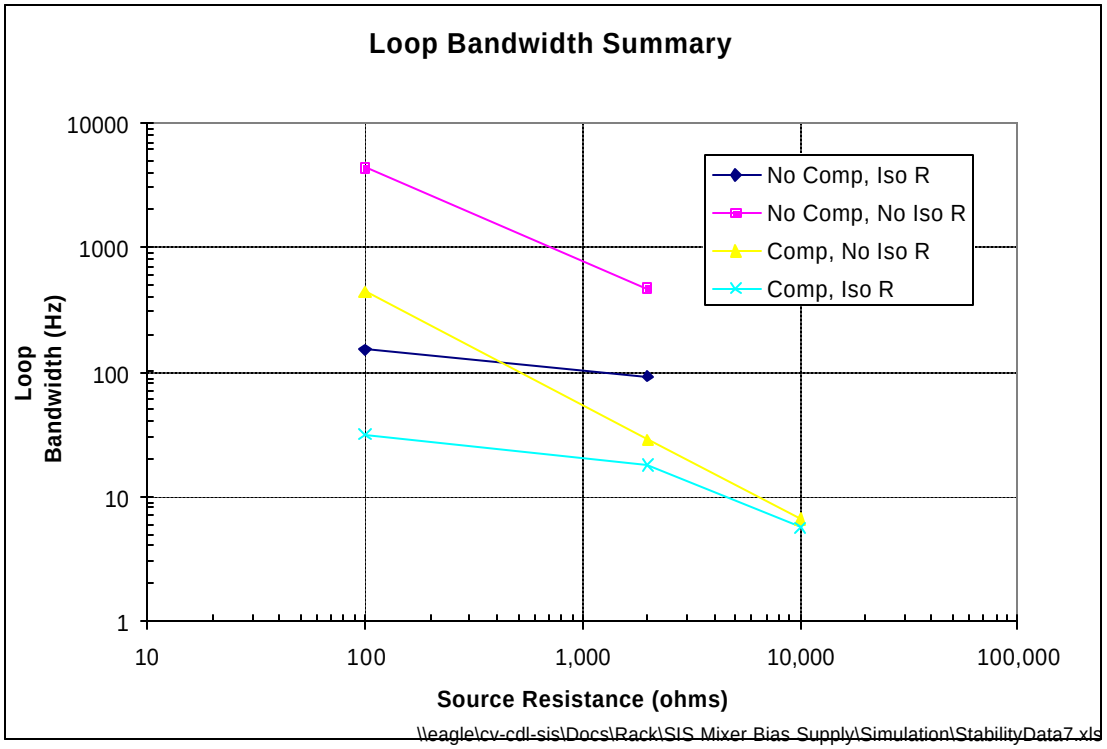

Figure 4: Loop Bandwidth Summary

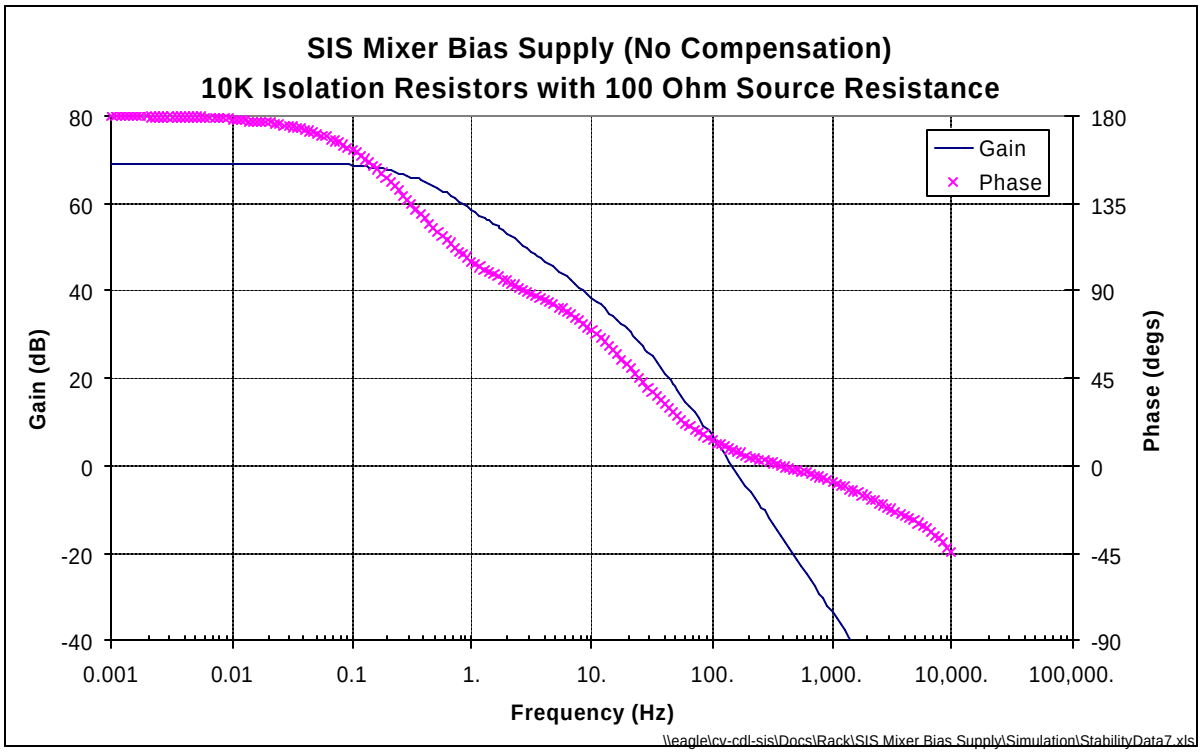

Figure 5: Bode Plot - No Compensation - 10K Isolation Resistors w/ 100 ohm Source

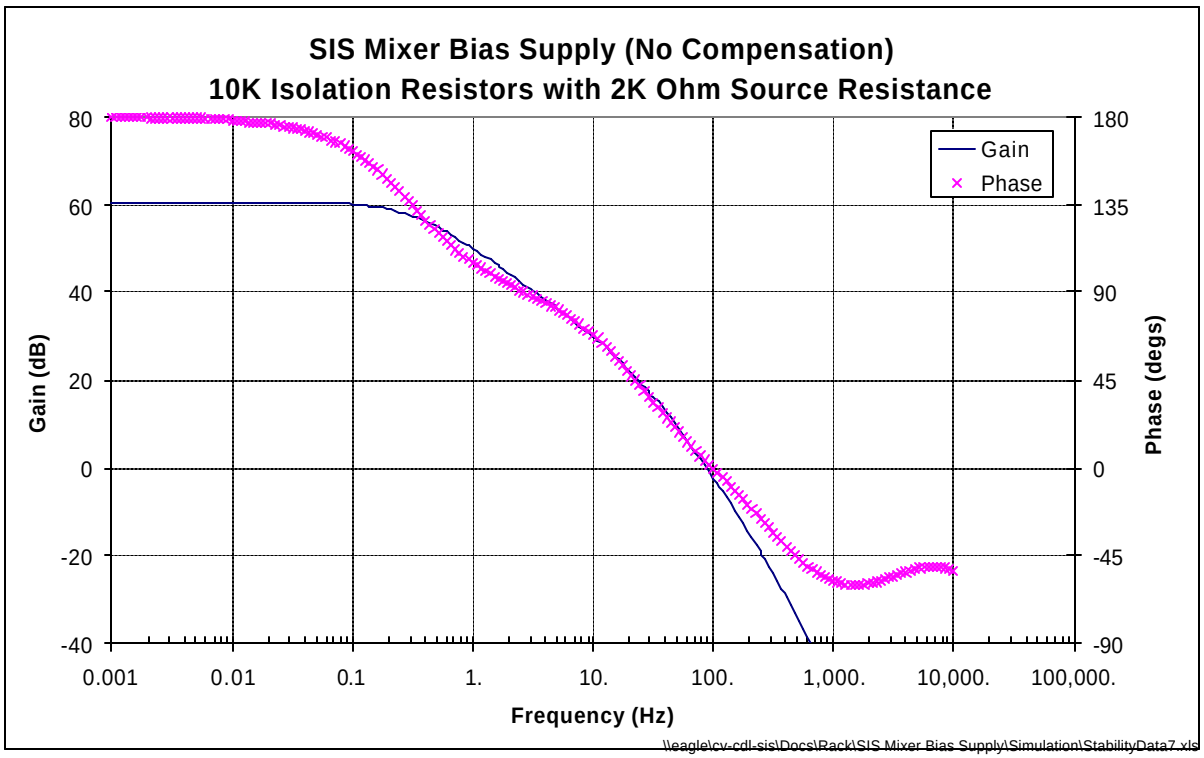

Figure 6: Bode Plot - No Compensation - 10K Isolation Resistors w/ 2K ohm Source

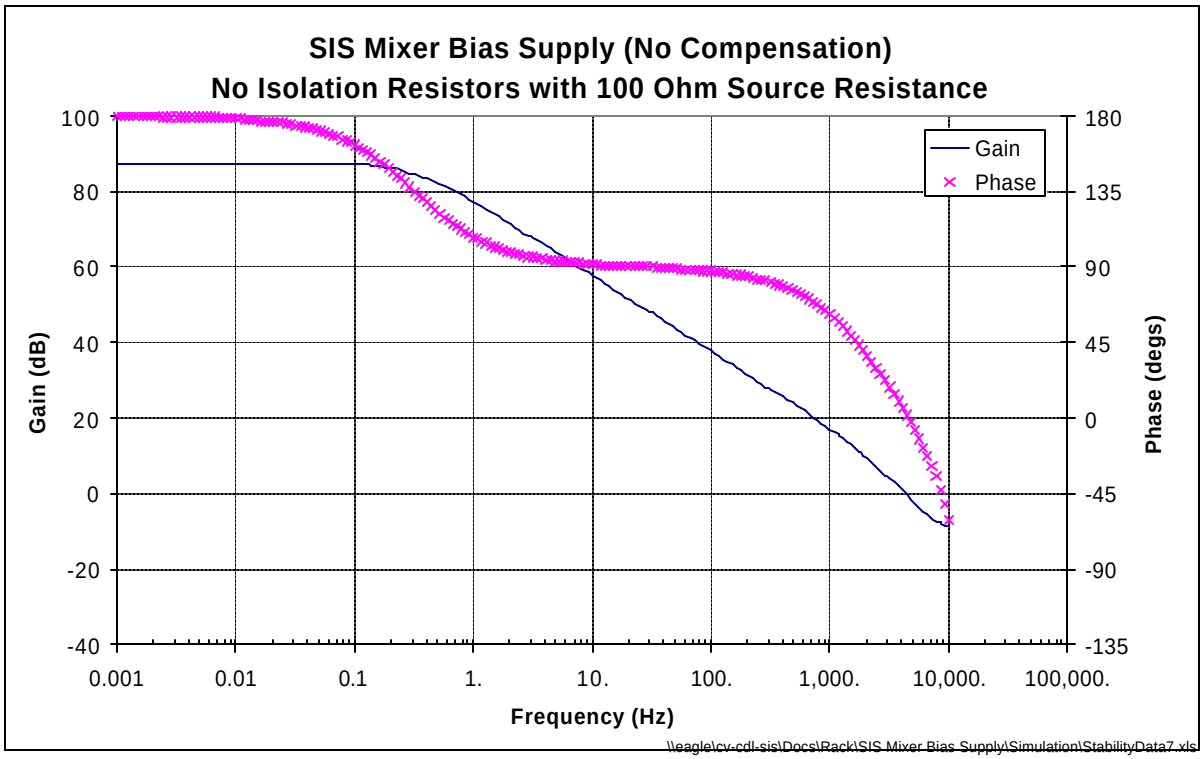

Figure 7: Bode Plot - No Compensation - No Isolation Resistors w/ 100 ohm Source

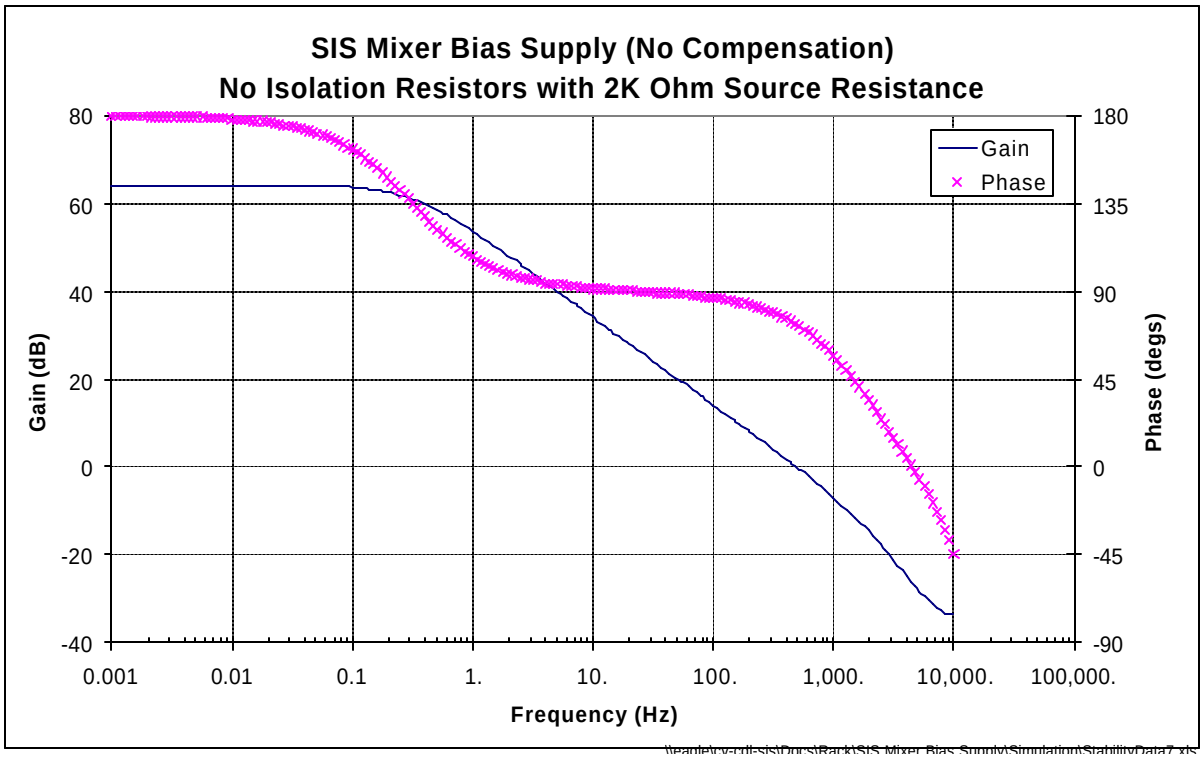

Figure 8: Bode Plot - No Compensation - No Isolation Resistors w/ 2K ohm Source

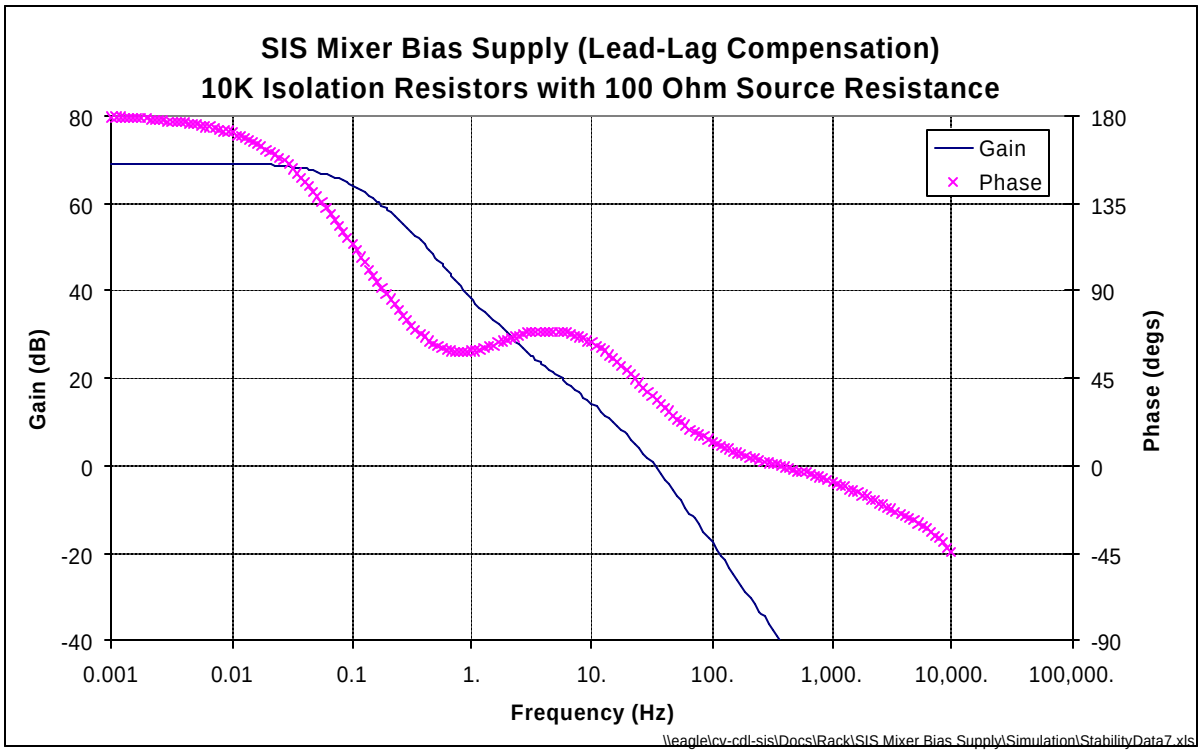

Figure 9: Bode Plot - Compensation - 10K Isolation Resistors w/ 100 ohm Source

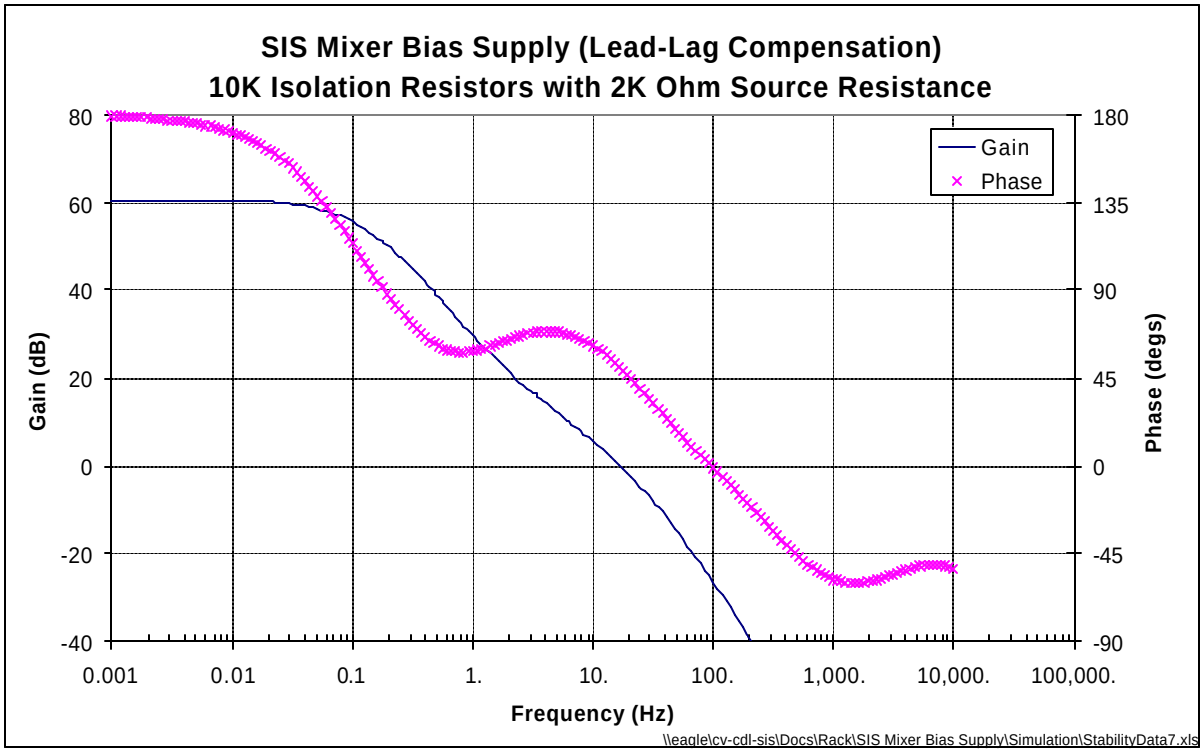

Figure 10: Bode Plot - Compensation - 10K Isolation Resistors w/ 2K ohm Source

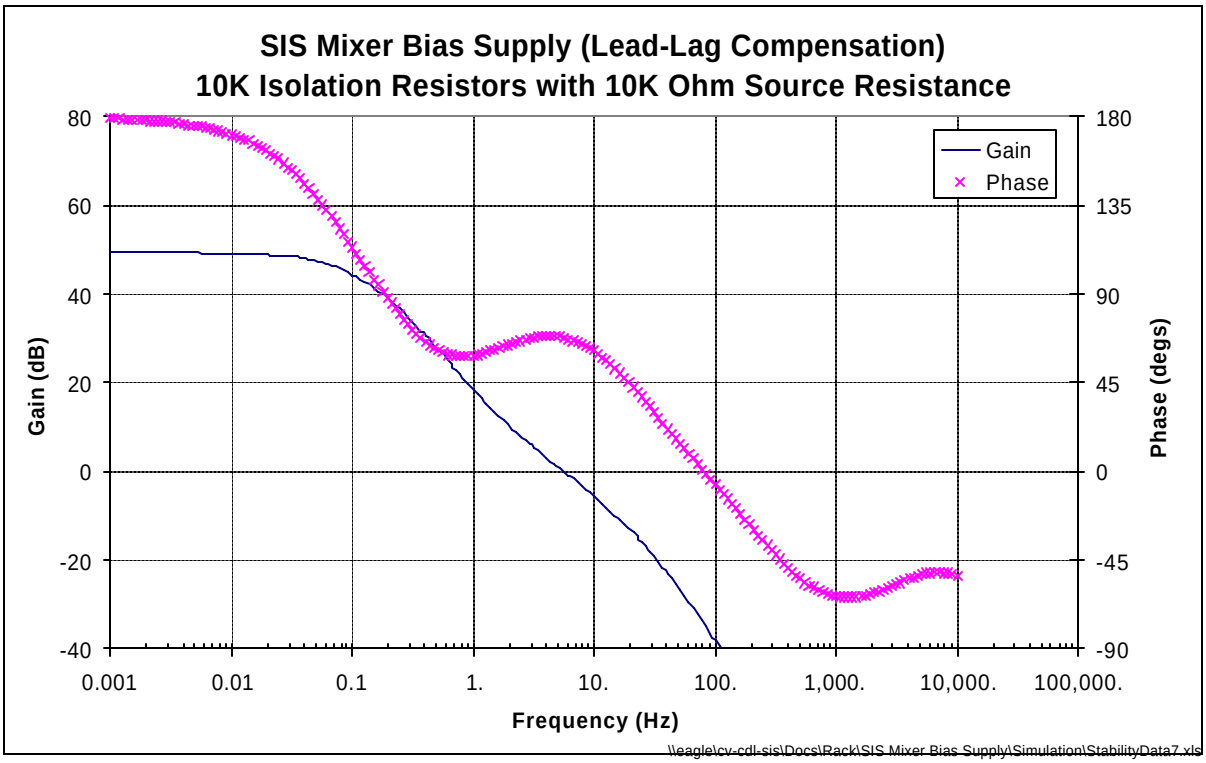

Figure 11: Bode Plot - Compensation - 10K Isolation Resistors w/ 10K ohm Source

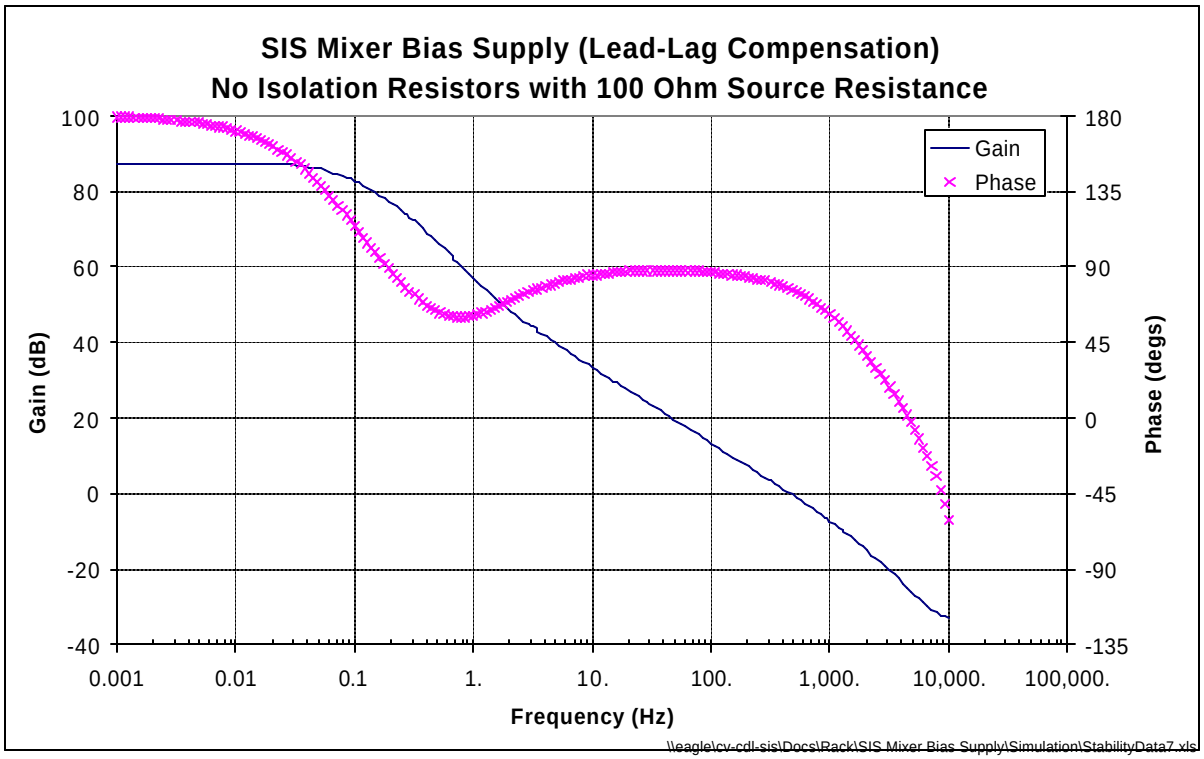

Figure 12: Bode Plot - Compensation - No Isolation Resistors w/ 100 ohm Source

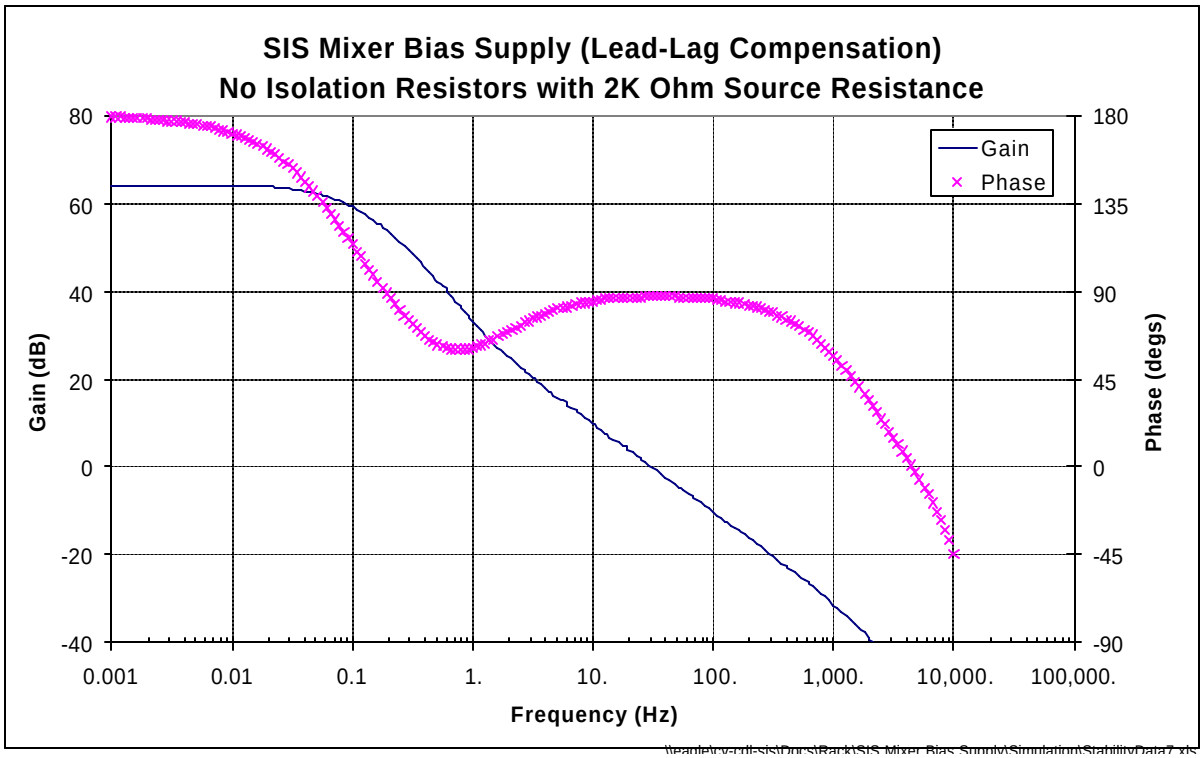

Figure 13: Bode Plot - Compensation - No Isolation Resistors w/ 2K ohm Source

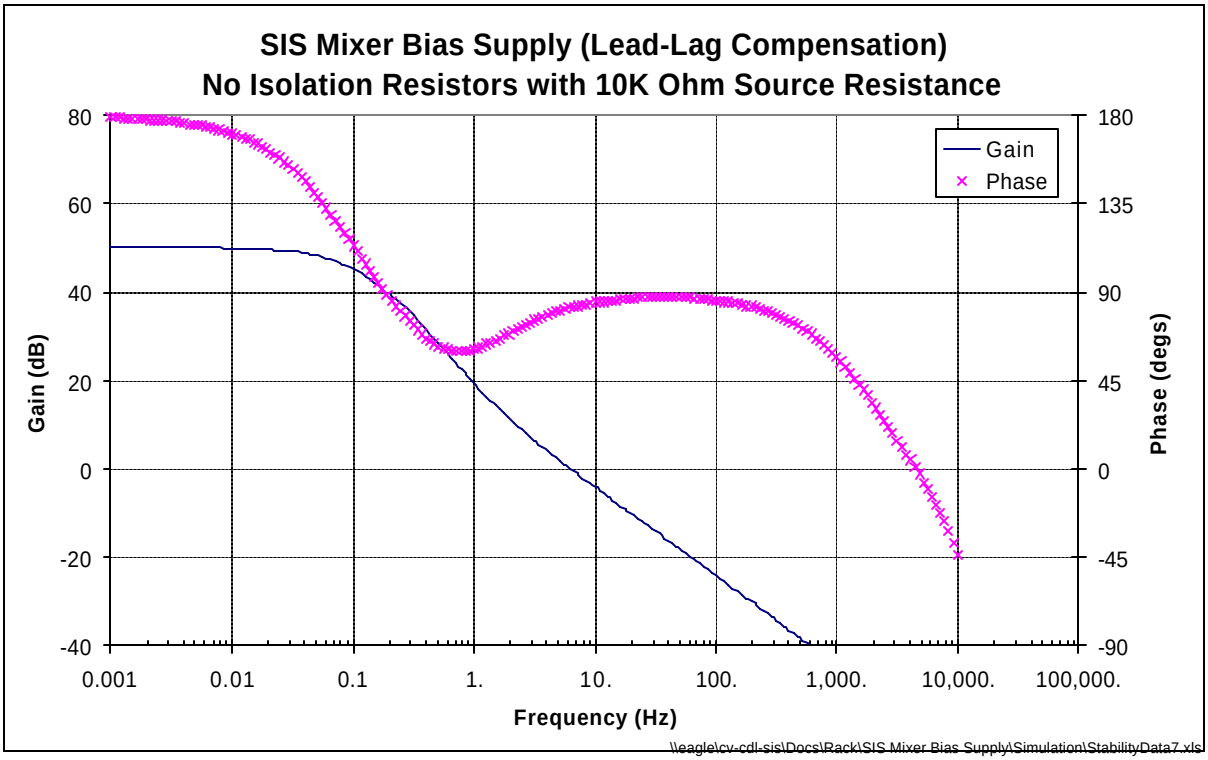

Figure 14: Bode Plot - Compensation - No Isolation Resistors w/ 10K ohm Source

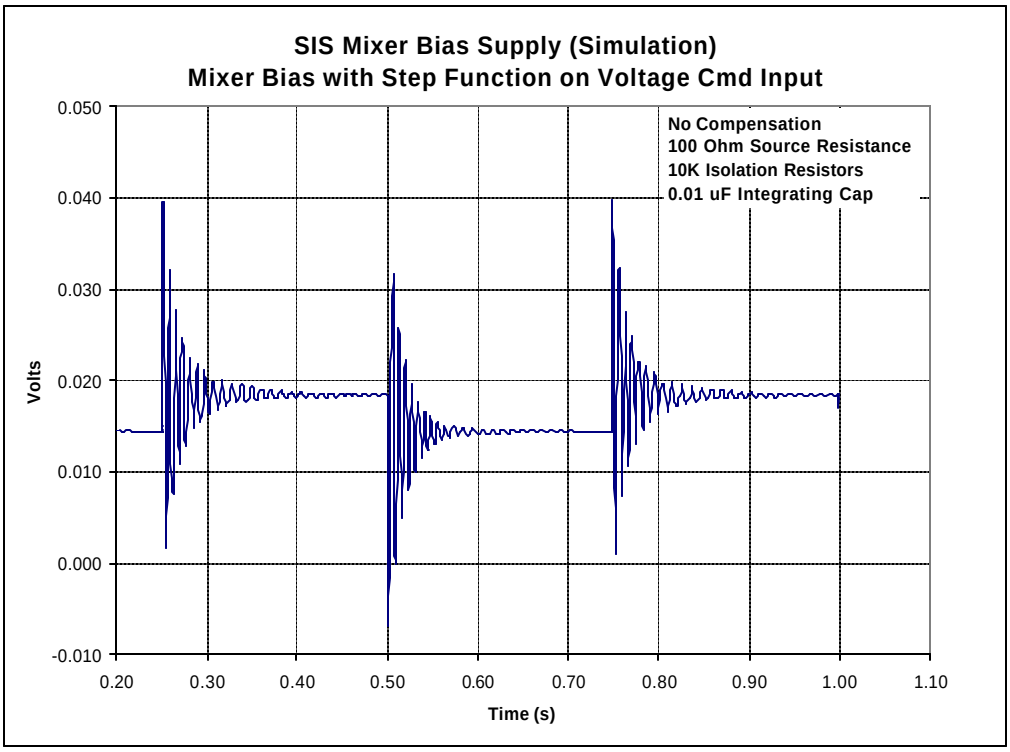

Figure 15: Time Plot (Simulation)- No Compensation - 10K Isolation Resistors w/ 100 ohm Source

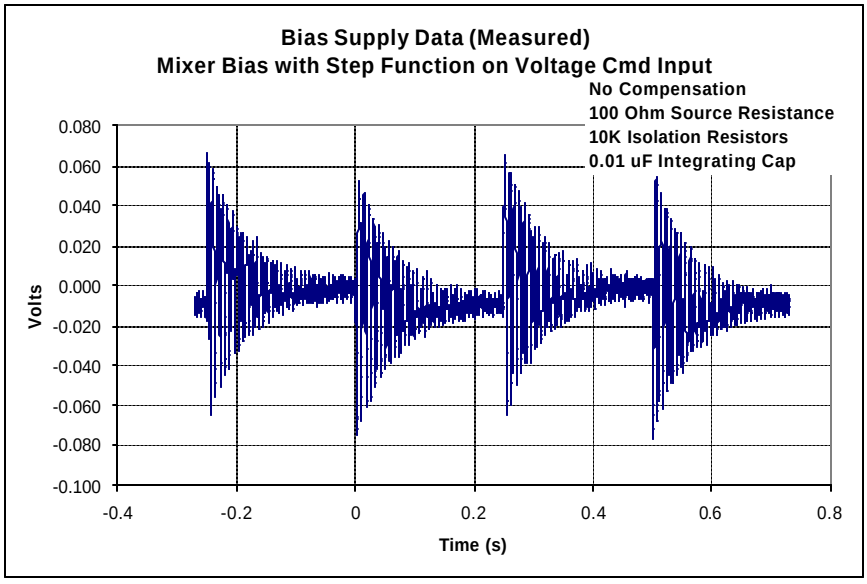

Figure 16: Time Plot (Measured)- No Compensation - 10K Isolation Resistors w/ 100 ohm Source

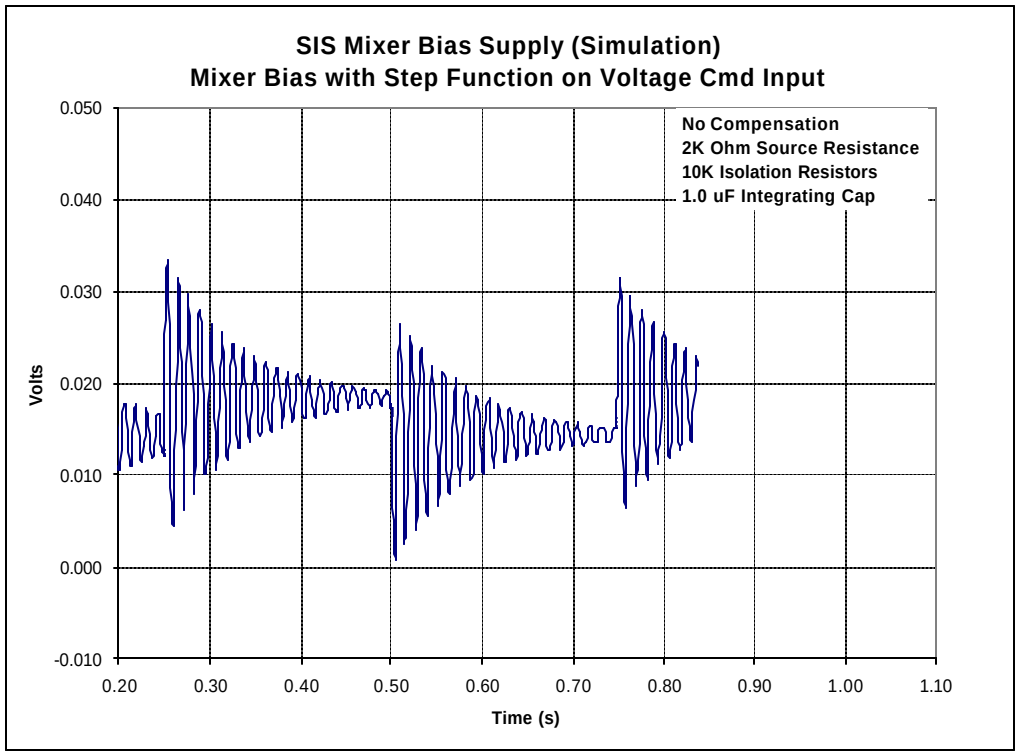

Figure 17: Time Plot (Simulation)- No Compensation - 10K Isolation Resistors w/ 2K ohm Source

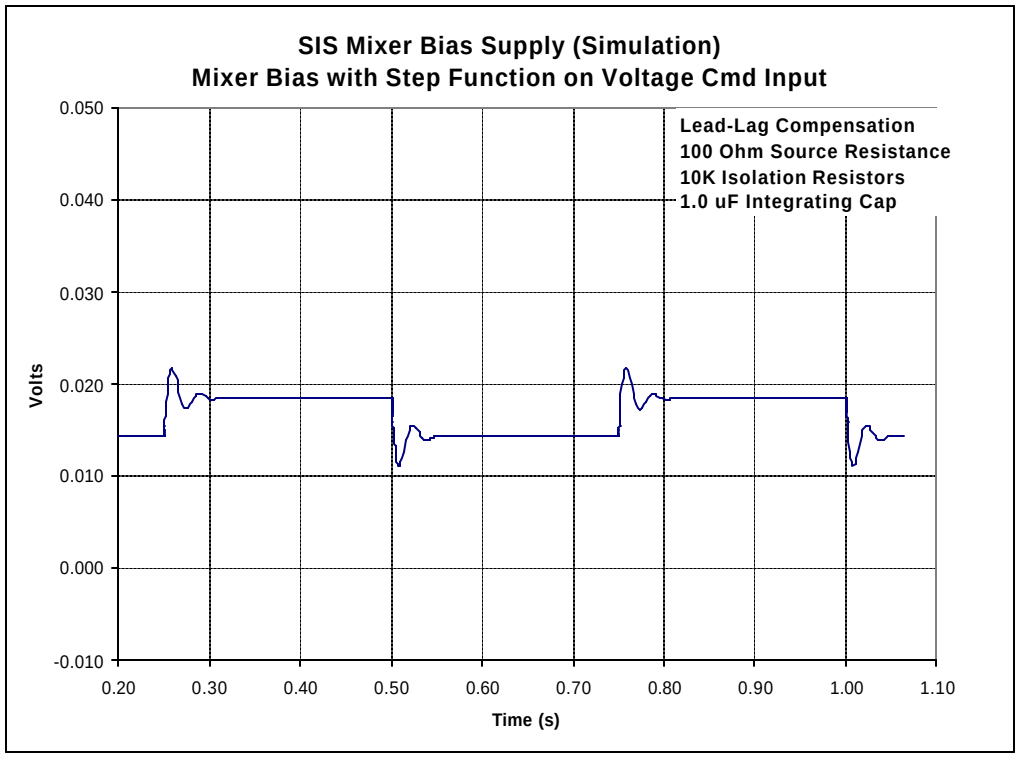

Figure 18: Time Plot (Simulation)- Lead-Lag Compensation - 10K Isolation Resistors w/ 100 ohm Source

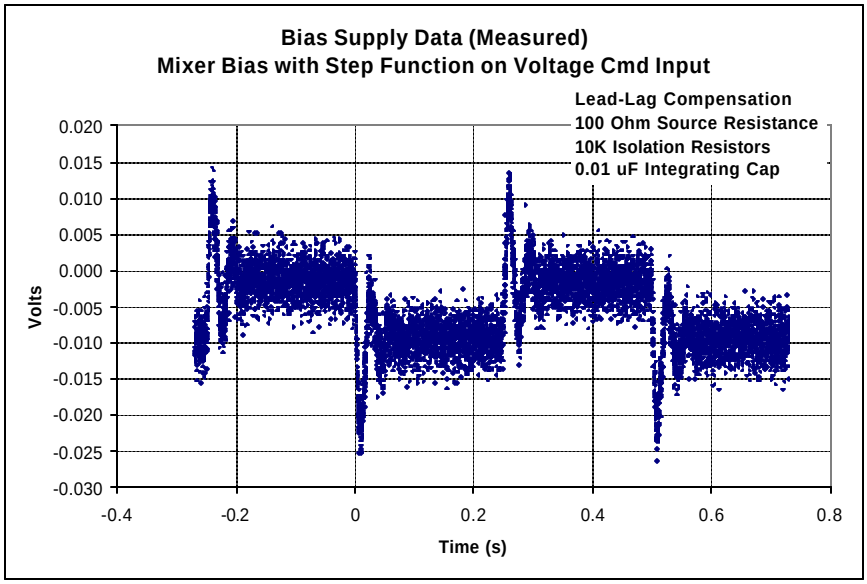

Figure 19: Time Plot (Measured)- Lead-Lag Compensation - 10K Isolation w/ 100 ohm Source

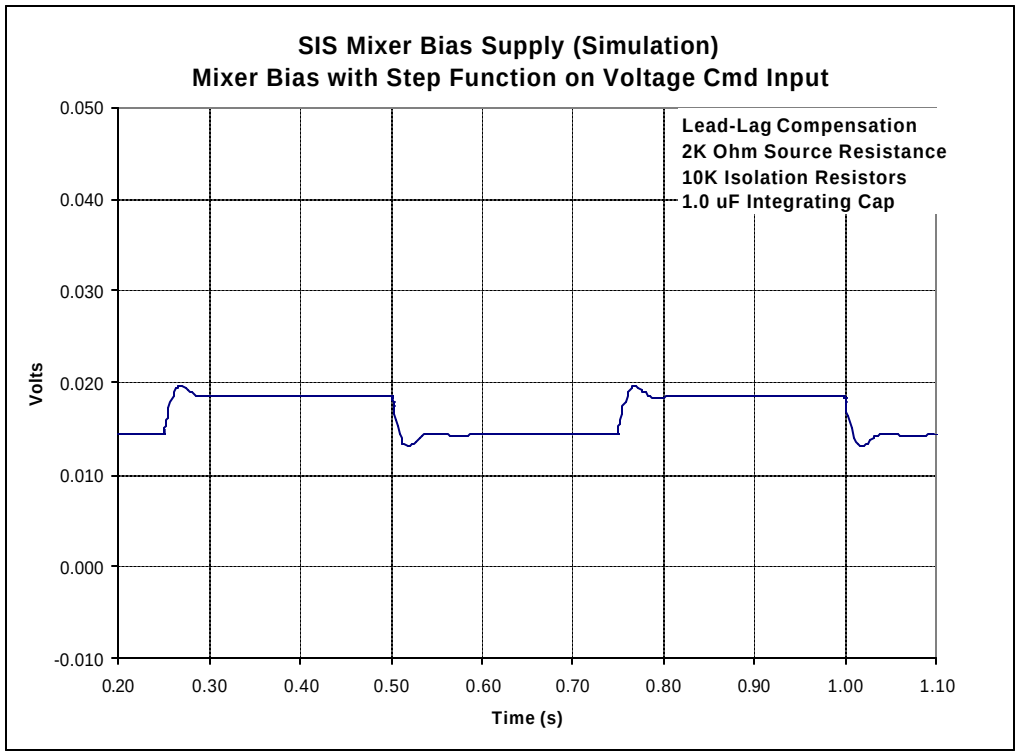

Figure 20: Time Plot (Simulation)- Lead-Lag Compensation - 10K Isolation Resistors w/ 2K Source

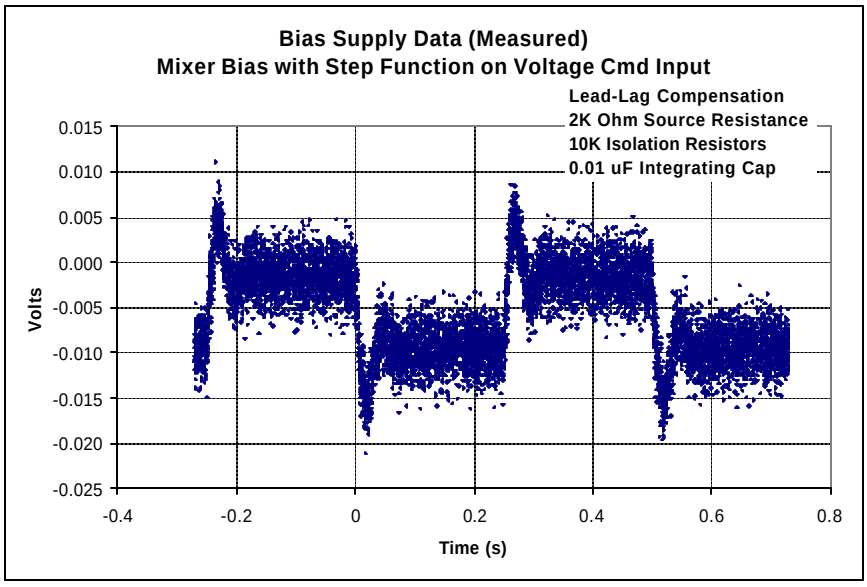

Figure 21: Time Plot (Measured)- Lead-Lag Compensation - 10K Isolation Resistors w/ 2K Source