Electronics Division Technical Note No. 189

Stability Analysis of SIS Mixer Bias Supply with 1K Ohm Isolation Resistors

29 November 2001

J. Effland

Summary

This memo analyzes the stability of the CDL's SIS mixer bias supply when it controls mixers with bias tees employing 1K isolation resistors. A revised lead-lag circuit with component values that optimize both phase margin and loop bandwidth is presented.

History

Recent SIS mixer bias tees built at the CDL include 10K ohm isolation resistors as shown in Figure 1 to protect the mixer junction from static discharge[1]. The mixers are powered by bias supplies, designed by A. R. Kerr[2], that provide switch selectable open- or closed-loop modes of operation. In closed-loop mode, the voltage feedback loop maintains a constant bias voltage at the mixer diodes. Kerr's circuit was never intended to operate with isolation resistors, and it occasionally oscillates when used with bias tees employing the 10K resistors, so a lead-lag circuit was added to that design to increase phase margins and improve loop stability[3].

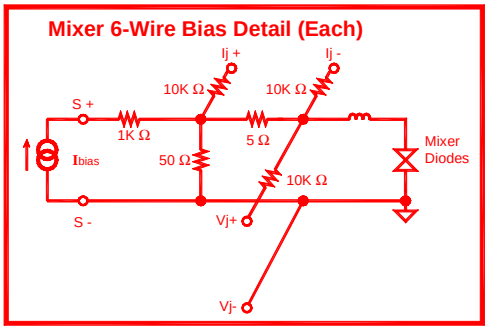

Figure 1: Present 6-Wire Bias Detail

The first lead-lag circuit modification to Kerr's bias supplies severely limited their usability because it remained in the circuit during open-loop operation, when it is not needed. This restricted the bias voltage sweep generator to unacceptably slow sweep rates because the lead-lag circuit limited the loop bandwidth to about 30 Hz. This limitation was corrected two months ago by slightly modifying the resistor values which allowed moving the lead-lag circuit out of the open-loop path.

Closed-Loop Bias Circuit

The closed loop bias circuit shown in Figure 2 is drawn with the simulation program "Electronics Workbench Version 5.12" that also provided all simulation results in this memo. The following subcircuits identified in the figure are discussed below:

Lead-lag circuit:	C28, R31, and R41
Integrating amplifier:	AR1 and C6
Isolation resistor:	R20
Source resistor:	R32

Figure 2 differs from the originally designed lead-lag circuit (Reference 3) because, as discussed previously, that design included the circuit in both the open- and closed-loop paths. It is now located between the integrating amplifier AR1 and the Open/Closed loop switch (not shown in Figure 2). There is another difference between the installed circuit and the design analyzed here: The installed circuit includes a 100K ohm resistor in series with the

[1] "The NRAO Type 2B 1-2 GHz SIS Bias-T," NRAO Electronics Division Technical Note # 173, A. R. Kerr and D. Boyd, 1996-02-15.
[2] "SIS Bias Supply, Type II," schematic from A.R. Kerr dated 1982-08-27.
[3] "Stability Analysis of SIS Mixer Bias Supply, " NRAO CDL Internal Memo, J. Effland, 2000-11-07.

(+) input of AR3, but this resistor is not needed because of the high input impedance of that op amp. R22 is used only for simulation to ensure convergence when the integrator circuit is analyzed.

Results

Figure 3 shows the phase margin and bandwidth of the bias supply drawn in Figure 2 as a function of R41's value when 10K ohm isolation resistors are used and the source resistance is 100 ohms. Figure 4 shows the results with the same isolation resistors driven by a source resistance of 2 K ohms. The points marked "Present Design" in both figures show the phase margin and bandwidth of the presently installed lead-lag circuit as summarized in Table 1.

Figure 5 shows the loop performance when all isolation resistors are 1 K ohm and the mixer is driven with a source resistance of 100 ohms. Figure 6 graphs the results for the same circuit when the source resistance is 2 K ohms. For the same loop bandwidth, the phase margins are considerably greater when 1 K ohm isolation resistors are used.

Table 1: Response of Presently-Installed Lead-Lag Circuit (R41 = 300K ohms, C28 = 5 uF)

Isolation Resistance (ohms)	Source Resistance (ohms)	Loop Bandwidth (Hz)	Phase Margin (degs)
10K	100	36	32
10K	2K	19	47

New Design

It is desirable for the mixer bias supply to operate with mixers employing bias tees with either 1K ohm or 10K ohm isolation resistors. But such flexibility requires loop bandwidth compromises compared to a design optimized entirely for 1K ohm isolation resistors. Consequently, it was decided to optimize the design by assuming that the bias tees contain only 1 K ohm isolation resistors. Table 2 summarizes loop performance for this case, and also includes loop performance when this circuit operates with mixers using 10 K ohm isolation resistors. The table shows that stability and bandwidth will be excellent for the new design driving 1 K ohm isolation resistors, but it will be only marginally stable when driving mixers with 10 K ohm isolation resistors.

Table 2: Response of Redesigned Lead-Lag Circuit (R41 = 50K ohms, C28 = 1 uF)

Isolation Resistance (ohms)	Source Resistance (ohms)	Loop Bandwidth (Hz)	Phase Margin (degs)
10K	100	89	12
10K	2K	50	15
1 K	100	210	42
1 K	2K	100	50

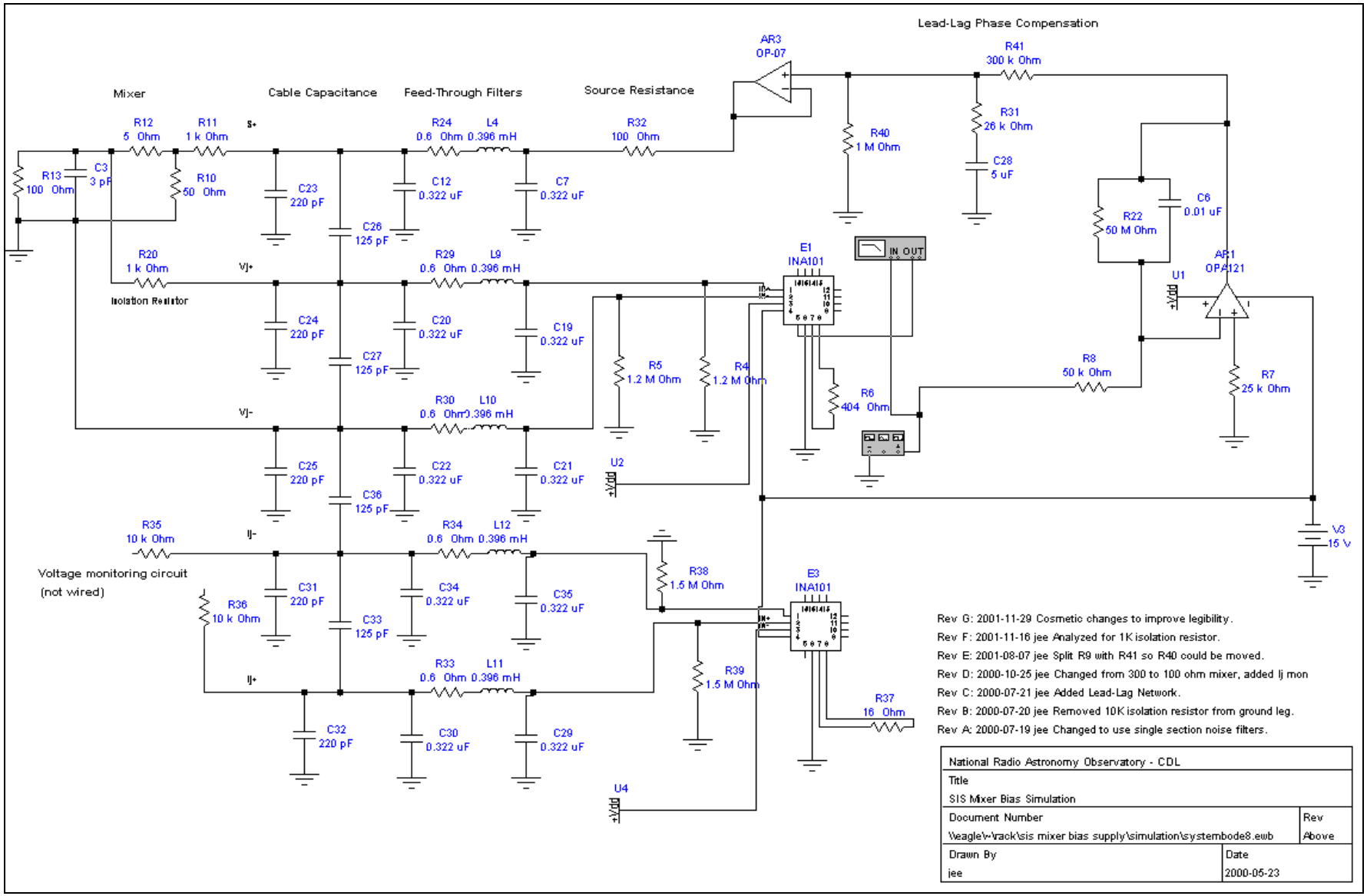

Figure 2: Circuit Analyzed by Electronics Workbench 5.12

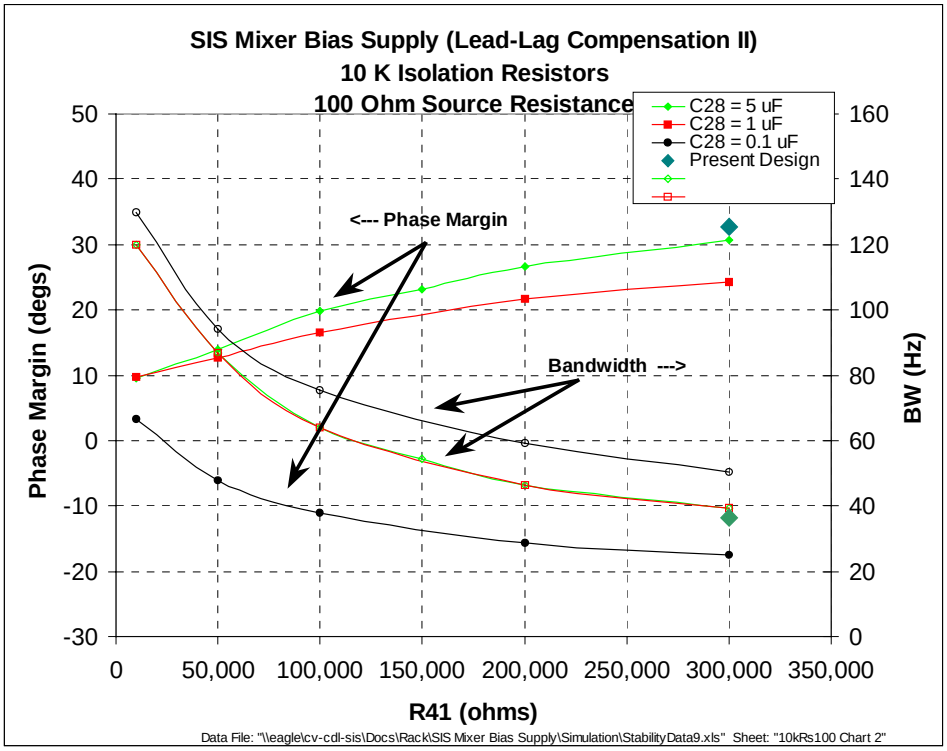

Figure 3: Loop Performance with 10K ohm isolation resistors and 100 ohm source resistance

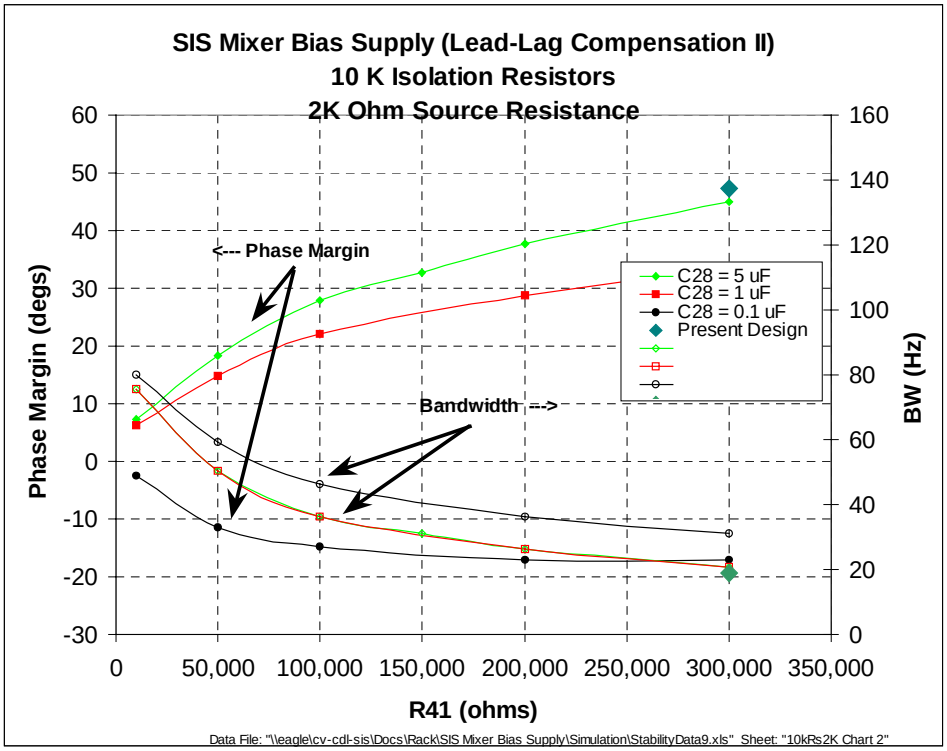

Figure 4: Loop Performance with 10K ohm isolation resistors and 2K ohm source resistance

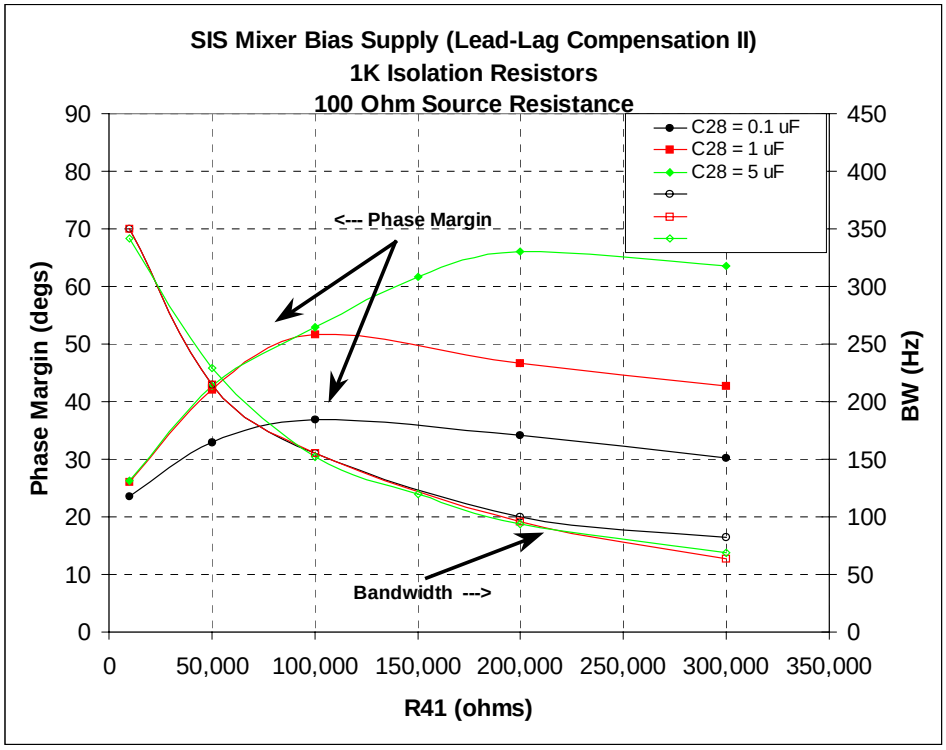

Figure 5: Loop Performance with 1 K ohm isolation resistors and 100 ohm source resistance

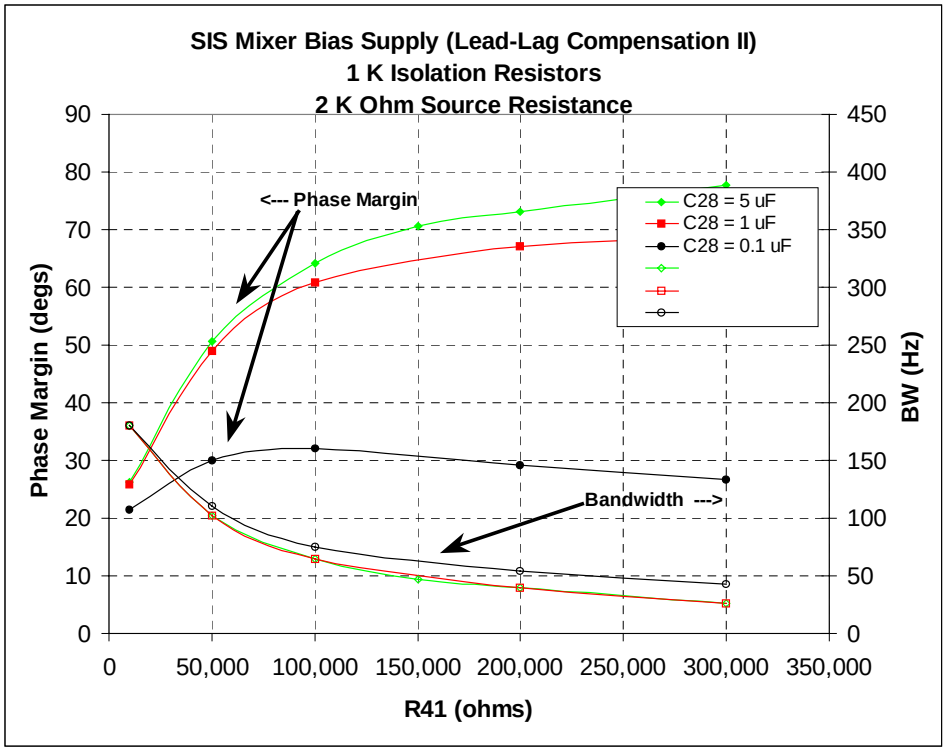

Figure 6: Loop Performance with 1K ohm isolation resistors and 2 K ohm source resistance