SIS Mixer Measurement System

Coax Switch Controller,

Refrigerator Controller, and

Chopper Wheel Controller

Design Document

2000-09-21

Version 1.72

Revisions

Table 1: Document Revisions

Revision Number	Date	Who	Details
1.0	1999-10-09	Jee	Initial
1.1	1998-10-29	Jee	Debrief for power supply PCB
1.2	1999-01-06	Jee	Included Design notes for future boards for switch control and power supply PCB's
1.3	1999-03-02	Jee	1) Further updating of as-build notes. 2) Added Computer I/O and Refrigerator Chassis
1.4	1999-03-25	Jee	1) Added comments about adding PA3 line. 2) Comments about replacing U5 in the power supply board.
1.5	1999-04-27	Jee	Added comments about rearranging the opto-isolator inputs so that the address decoders sink current from the opto-isolators.
1.6	1999-06-01	Jee	1) Comments on rewiring of ISO1C to active low on the power supply board 2) Comments on rewiring of ISO2 for active low switch control. 3) Comments on white wire from U22-2 to U23-2
1.6	1999-08-04	Jee	Added Chopper wheel section
1.7	1999-10-06	Jee	Revised Chopper wheel section to include National Instruments counter 1 and counter 0 programming
1.71	2000-01-17	Jee	Revised Chopper wheel section. It no longer directly provides the CONVERT pulse to the A/D converters.
1.72	2000-09-21	Jee	Added measured timing data to Chopper wheel section.

Contents

List of Attachments

List of Figures

List of Tables

1. Introduction

This document provides hardware design and assembly details for the Coaxial Switch Control chassis and the Refrigerator Control chassis, which is part of the SIS mixer measurement system. The Coaxial Switch Control chassis controls the following functions:

1. Sets and resets the coaxial IF switches in the dewar
2. Turns the noise source on and off
3. Turns the 4K heater on and off

The Refrigerator Control chassis provides the following functions:

1. Connects the computer's analog and digital interface board, a National Instruments AT MIO DE10, to the rest of the equipment via a National Instrument's SCB 100 interface box, which is mounted inside the chassis.
2. Controls the Dewar heater, vacuum valve, and refrigerator.
3. Interfaces the Haistings Pressure gauge via a VLBA sensor card.
4. Routes digital address lines to the Coax Switch Controller

Three printed circuit boards reside inside the coaxial switch module:

1. Switch Driver contains the driver transistor and associated circuitry to control the coaxial switches in the dewar.
2. Switch control contains the logic to decode the computer addresses and send the proper commands to the switch driver PCB.
3. Power supply provides the +/- 18V, +15V, +5V, and +30V levels. The +30V is used to power the 28V noise source. This board also contains logic to decode the noise diode and heater commands from the computer.

The overall schematic is included as Attachment 1. Each of these boards is described in the following sections.

2. Switch Control PCB

The switch control PCB, designed by Kirk Crady, decodes the computer addresses into commands that are sent to the switch driver PCB. The top-level schematic for this PCB is page 7 in the attached schematic pages and the underlying circuits are pages 3 to 7. Kirk's design was modified to reduce the component count by replacing the discrete NAND gates with a 74LS279 and the discrete pull-up resistors with resistor arrays.

The address map for the computer interface is defined in the software design document. Data lines PA2 to PA0 should first be commanded to set or reset the proper coaxial switch, after which address lines DIO3[1] to DIO0 should be set to 1101 to latch the switch command into U1.

[1] Bit DIO3 is used for address enable. That is, bits DIO0 to DIO2 and PA0 to PA2 should be set to the desired address, then DIO3 can be strobed to latch the address. In practice, all address lines are set simultaneously and dwelled for a few 10's of milliseconds.

Circuit operation is exemplified as shown by referring to page 6 of the schematic. The set command can be effected from either the computer (via the SET_CMD) or manually from SW-2 on the front panel. SW-2 is ganged with another pole in the Switch Driver circuit. U26 debounces and latches the SET and RESET commands, which are sent to reed relay U23 and to the front panel LED indicator. The reed relay contacts are connected in parallel across the switch contacts in the Switch Driver circuit to control the switch.

The Switch Control PCB layout is shown as Attachment 2.

2.1 Switch Control PCB Assembly Notes

1. The holes in the printed circuit boards are not plated-through, and it is necessary to solder components to both sides of the board. Some of the IC pins must be soldered to the IC pads on the component side of the board, which is complicated because one must solder under the IC sockets. An approach that works is to raise the IC sockets above the board slightly, and use a soldering iron with a fine tip. The tip point should be filed so its diameter is equal to the width of the IC pins. The tip should be bent slightly so the soldering iron can clear adjacent sockets when soldering.
2. There are about 10 via's that must have wires soldered to them from both the component and solder side of the board.
3. Wire from U22-2 to U23-2 on solder side of board.

2.1.1 Design notes for future boards

1. Change 25uF input capacitor on 5V line to 10uF tantalum.
2. Solder side and component side were switched by WWW.
3. On all connectors, identify pin 1 on silkscreen
4. Move IC reference designators out from under chips.
5. LS08'S are 14 pins, rather than 16 pins.
6. V_{cc} trace to U26, U33, … is not connected to V_{cc}.
7. Connectors J3 and J4 are too close.
8. Route PA3 to the Refrigerator controller to control the state of the noise diode and heater.
9. Track from U22-2 to U23-2 on solder side of board

3. Switch Driver PCB

The legacy design of the switch driver PCB was retained, which is essentially A. R. Kerr's design sketched in his lab notebook as revised and dated 1984-02-21. This board contains circuitry to drive six dewar switches, but since the rest of the design can only control four switches, two of the sections on the board are not populated. The NPN driver transistors used in the working version of this board, 2N2219's are also becoming obsolete and will be replaced by 2N4401's.

The schematic is shown on Pages 8-11 of Attachment 1. The PCB component placement diagram is shown on Attachment 3. Only the lower left-hand corner of the component placement diagram is annotated, and only with component values, since each section has identical values.

Based on experiments with D. Koller dated 1999-05-25, the values of the integrating capacitors in the switch driver circuit were changed from 0.1 μF to 0.049 μF. This doubles the slew rate and improves the switching reliability of the switches in the Mixer 1 Dewar used with backshort-tuned mixers.

4. Power Supply PCB

The power supply provides regulated +/- 18V[2], +15V, +5V, and +30V levels. The +30V is used to power the 28V noise source. This board also contains logic to decode the heater and noise source commands from the computer. The schematic is shown on Page 2 of Attachment 1.

The legacy LAS-15U and LAS-18U variable-voltage regulator IC's are obsolete, and have been replaced by LM317's and LM337's.

Opto-isolators partition the 5V computer logic levels from the higher drive voltages. They use Darlington output stages that handle about 30 mA of collector current with only about 1 mA of LED current.

The original circuit used a 2N2905 discrete transistor to drive the noise source, but these are becoming obsolete, so a 2N4403 was used as a replacement. By "OR"ing three of the opto-isolator outputs together, the noise diode current[3] can be obtained from either the front panel switch, digital control, or the 10V pulse input.

Attachment 3 shows the PCB layout for the Power Supply.

4.1 Power Supply PCB Assembly Notes

1. The pads around all voltage regulator pins on the solder side of the board have small protrusions near their edges. It may be necessary to scratch the copper between these pads.

2. The LM317 and LM337 voltage regulators must be insulated from the board. Use mica insulators and heat-sink compound.

3. The board will use plated-through holes – no soldering is required on the component side.

4. R7 is a potentiometer mounted on the chassis front panel. The wiring for the "Load Heater" connection is made directly to this potentiometer, but the common connection on the potentiometer should be connected to the ground terminal on the PC board.

5. Lift pins and add white wires as required to connect U5 to ISO2C and ISO2A with SW5 bypass as shown on the schematic.

6. ISO-1: Changes to make noise source drive from active low.
   - Lift Pins 5 & 6
   - Wire from PCB hole pin 5 to IC pin 6

[2] Although annotated as ±18V, the actual voltage used is ±17.5V.

[3] HP specified that the current for their 346A/B noise diodes is 60 ma peak and 30 ma average when the source on. The HP 436C noise diode has a peak current requirement of 45ma.

- Wire from IC pin 5 to +5V

7. Top-view pinouts of the 2N4401 and 2N4403 transistors is shown in Figure 1:

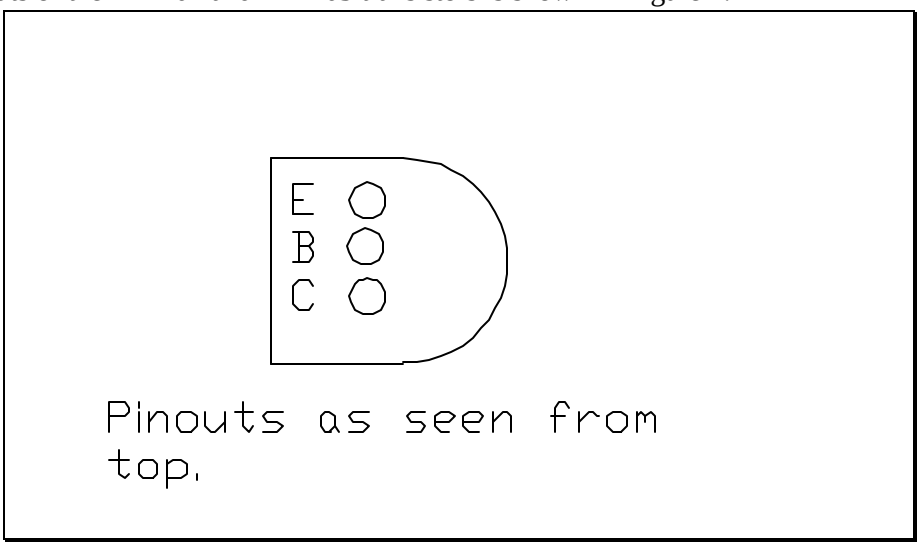


Figure 1: Pinouts of the 2N4401 and 2N4403

4.1.1 Design notes for future boards

1. Holes for ±15V voltage converter are wrong.
2. Swap tracks for +/- input voltage on voltage converter
3. Holes diameters for 78XX regulators are too large.
4. Clearance of 78XX holes is tight.
5. Clearance around all solder pins is too small.
6. Mounting holes for voltage converter are wrong.
7. U4 R1 labeled incorrectly on silkscreen – should be R3.
8. R20 (2W resistor) holes too small.
9. Change (+) sign on C13 to other lead.
10. Via pads can be smaller
11. Pins 3 and 4 for both optoisolators are reversed.
12. U5, the 74LS138, is not a latching device, so the noise diode and dewar heater command addresses must remain static when needed. Replace this with a 74LS259, which is a latching decoder. It will also be necessary to add another address line (PA3), to set the state of the line (either set or reset). This address line will need to be added to the Coax Switch controller, too.
13. The 5V regulator gets hot, even with a small heat sink. If redesigned, allow sufficient board space for a larger heat sink.
14. Since LS totem-pole output circuits can sink more current (4 mA) than they can source (0.8 mA), rearrange the opto-isolator outputs so that current flows from +5 V, to a dropping resistor (1.5K) to the address decoder outputs.

5. Computer I/O and Refrigerator Chassis

5.1 Purpose

The computer I/O and refrigerator chassis provides the following functions:

1. Interfacing between the National Instruments I/O card and external signals via the National Instruments 200B ?? interfacing box.
2. Manual and computer control of the refrigerator and vacuum valve between the Dewar and vacuum pump.
3. Interface card to read Dewar pressure using a Haistings gauge and convert this pressure to a voltage using an old design of the VLBA "Front End Sensor Card". This card can read a number of pressure gauges, but only section D is used for the SIS Dewar.

5.2 General Notes

1. Modify the VLBA Sensor card to remote R3 and R15 to the rear panel of the chassis.
2. Add a retainer clip to the power supply connector. Do this for the existing unit, too.

5.3 Multiplexer Controller

The following serve as assembly notes:

3. +/- 15V supply lines for ADG407 are reversed. Cut tracks and white-wire to correct.
4. Scratch tracks to move U2-1 from U1-14 to U1-12. This changes the address of Valve Open, *etc*. from 001 to 011.

6. Chopper Wheel Trigger Controller

6.1 Purpose

The chopper wheel trigger controller sends trigger pulses to the National Instrument I/O board that are synchronized to the chopper wheel.

6.2 Circuit description

Two optical interrupters installed on the chopper wheel provide a "Full Clock" and "Half Clock" pulse trains. The Full Clock is a pulse that occurs each time the beam from the receiver passes through either the open and closed sections of the wheel. The Half Clock pulse train only occurs when the beam passes through the open (or closed, depending on final implementation details) sections of the wheel. The National Instruments' card is configured so that trigger pulse from the Trigger Controller triggers other counters on the National Instruments' card. These counters provide a CONVERT pulse to the A/D converters on the National Instrument's card which initiates the conversion. The results of each A/D conversion is stored in a memory location, which is later retrieved and

processed. Using both the full and half clock pulses ensures that the first element in the memory array is noise power from, say, the hot load.

To reduce the variance in the data, more samples are required for averaging. Initial attempts to increase wheel speed to achieve additional samples were unsuccessful because wheel resonances cause stalling at speeds above about 12 revolutions per second. To increase the sample count for a fixed wheel speed, the National Instruments card was configured to acquire multiple samples for each trigger pulse received from the chopper wheel.

As shown in Figure 2, internal counters on the National Instruments card are configured to generate multiple pulses for each trigger pulse from the chopper wheel. Counter 1 derives its clock from the 100 kHz clock on the National Instruments card, and is gated by the trigger pulse from the chopper wheel. This counter is programmed using National Instrument's driver as a "Retriggerable Pulse Generator" that outputs pulses each time the trigger input changes from low to high. The start time and duration of the pulse generated by this counter is defined in terms of 100 kHz clock pulses by the software.

Counter 1's output is routed to the gate of Counter 0, which is configured using National Instrument's driver as a "Pulse Train Generator" to output a pulse whose high and low duration, in units of the 20 MHz clock, is also set in software. National Instrument's Driver prevented using the internal 100 kHz clock for counter 0, but the 20 MHz clock works better because it has finer resolution. The output of Counter 0 is defined as N pulses, each with a period of 10 μs, which is about the reciprocal bandwidth of the National Instruments analog section. This allows N statistically independent samples to be averaged each time a trigger is received from the chopper wheel.

Figure 4 shows the signal routing for the chopper trigger. Triggering commences when the program sets the DIO-7 line high on the National Instruments card. This enables trigger outputs from the chopper trigger, which are fed to the gate input on Counter 1 on the National Instruments card. The output from Counter 1 is routed, *via* wires in the SCB-100 interface in the Refrigerator Controller chassis, to the Gate of Counter 0. The output of Counter 0 is fed, via internal connections on the National Instruments card, to the CONVERT line of the digital to analog converter on that card.

Figure 3 shows measured chopper timing pulses (the CONVERT line) to the D/A converters vs. the output from the square law detector. The timing pulses are not resolved in this plot, but there are 256 timing pulses present during the hot load state.

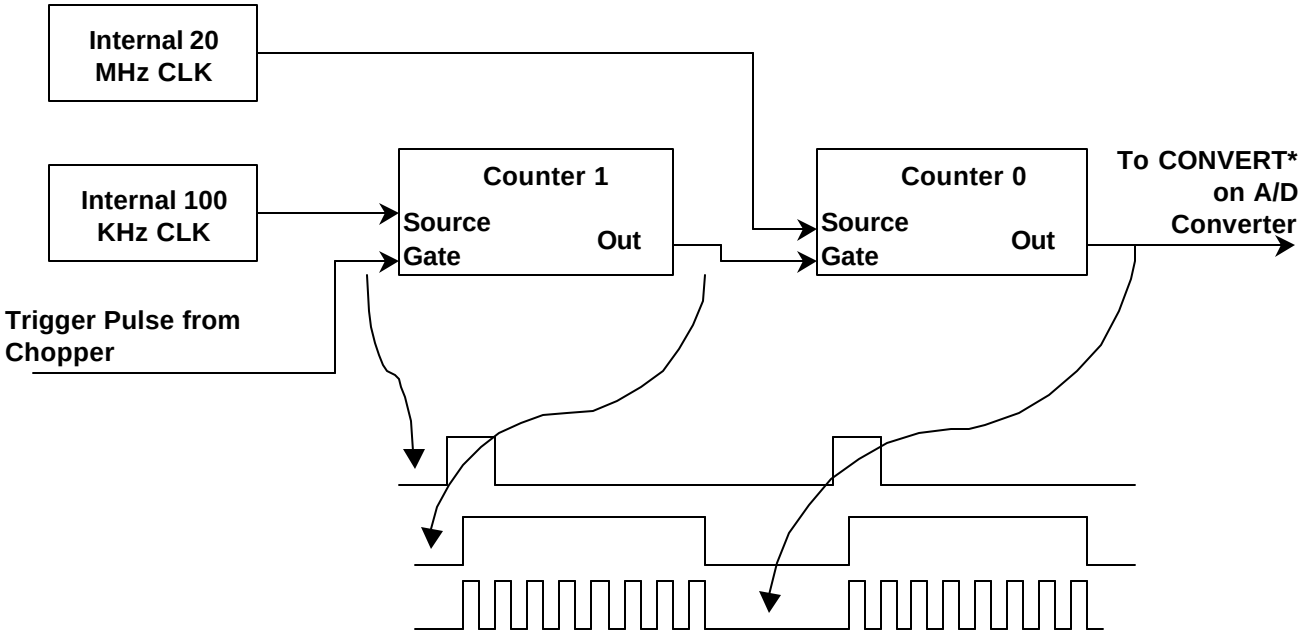


Figure 2: Triggering Circuit for Chopper Wheel A/D Converter

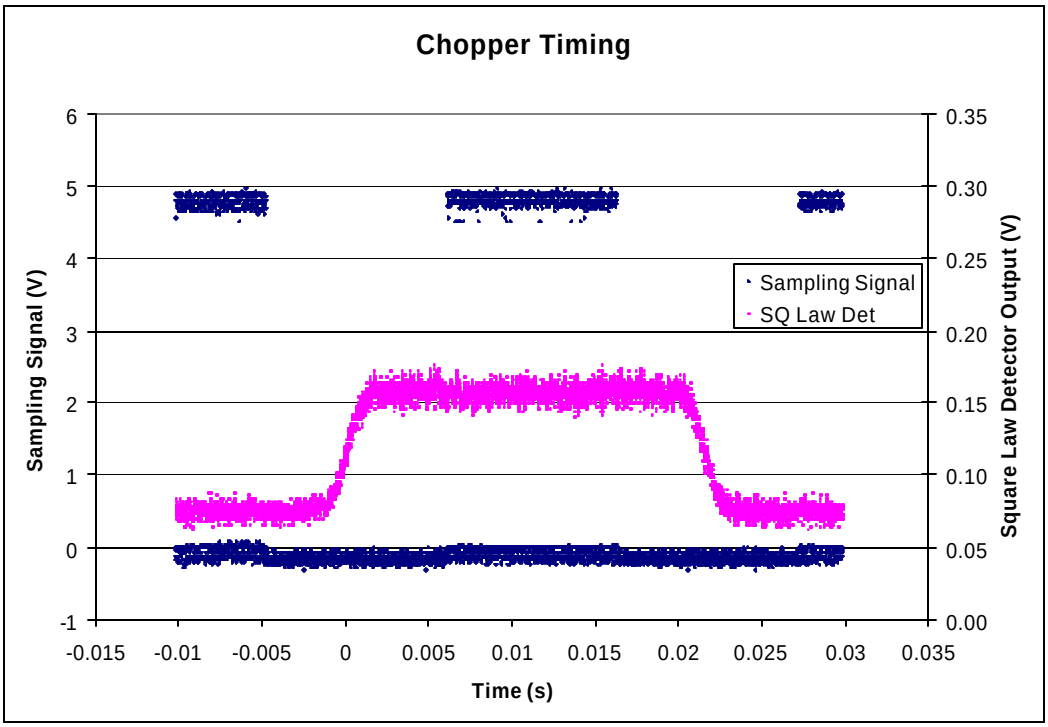


Figure 3: Oscilloscope Data for Chopper Timing

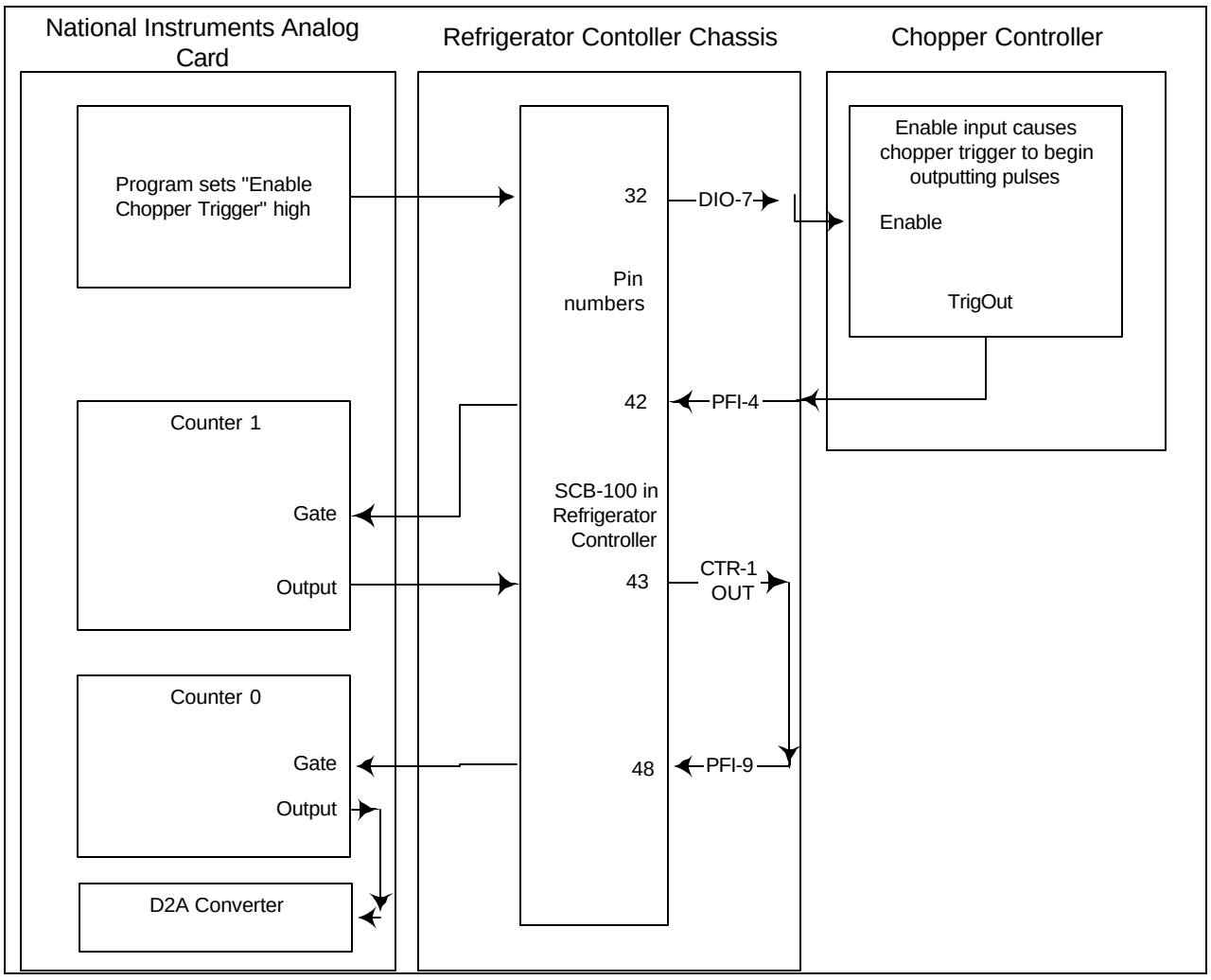


Figure 4: Chopper Trigger Signal Flow Diagram

6.3 Design Notes for Final Trigger Circuit

Optical Interrupter Stage

This stage consists only of the two optical interrupters, and four resistors. R1 and R3 limit the current through the interrupter LEDs, while R2 and R4 limit the current through the interrupter collector-emitter junctions.

The clock pulses that originate from the optical interrupters are very noisy and are do not settle at clean logic levels. One possible way of smoothing out the pulses may be to insert a capacitor between each output of this stage and ground.

Comparator Stage

Due to the noise on the outputs of the interrupters, they are unable to directly drive TTL logic. Two comparator circuits clean up this signal considerably. The signal voltage level at which each comparator produces a high output can be adjusted through POT1 and POT2. The circuit was successfully tested with the reference voltage (the voltage on pins 5 and 7 of the comparator IC) at 3 volts. The addition of R7 and R11 between the

outputs and the reference voltages of the comparators provide hysteresis. These comparators are configured to be inverting, so that a positive pulse is generated whenever the optical interrupters are off (i.e. they are over a dark spot or a hole).

Logic Stage

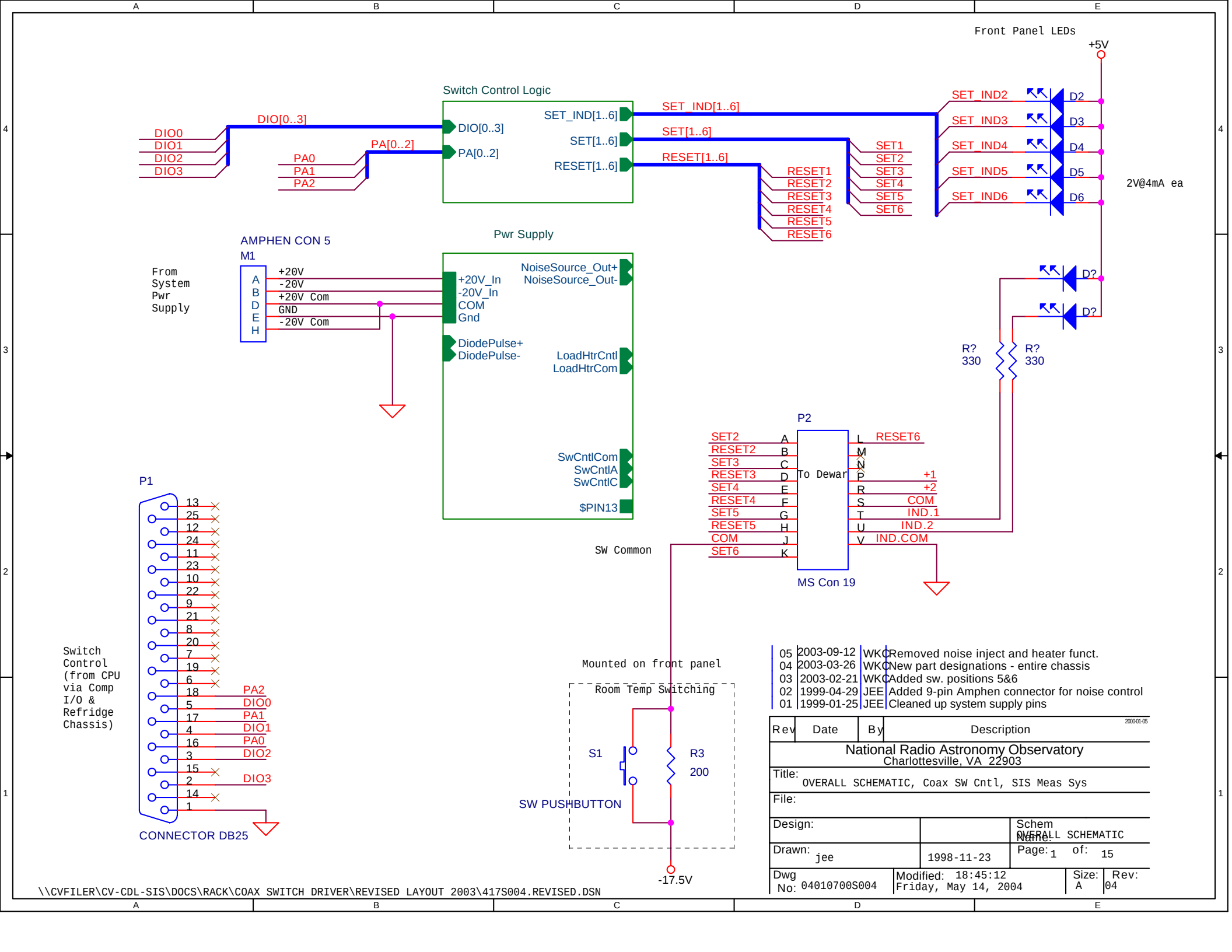
In order to assure that NI-DAQ card receives the first pulse during a half clock pulse, a flip flop clocked on the half clock signal is used. The flip flop passes the enable signal (from the NI-DAQ card, DIO7 or pin 32 in breakout box, controlled by software) to an AND gate whenever a half clock signal begins. When the enable signal is high, and it has been passed to the output of the flip flop (Q, or pin 5), it allows the full clock signal to pass through to the CONVERT line (connect this to PFI2/CONVERT*, or pin 40 in breakout box).

To ensure that only full pulses reach the CONVERT line, the half clock signal ***must*** lead the full clock signal by an amount of time equal to the propagation time through U2A (the flip flop) and U3A (the AND gate). This is probably best achieved by positioning the interrupters such that the half clock pulse occurs just slightly before the full clock pulse.

NOTE: This circuit must be grounded with DGND in the breakout box. This is available on pin 33.

R13, a 1K resistor between ENABLE and ground, is necessary to pull the ENABLE line down to ground when it is in the inactive (tri-state) mode. Without it, the flip flop assumes the ENABLE is high, and starts sending CONVERT pulses.

Attachment 1: System Schematic



Rev	Date	By	Description
05	2003-09-12	WKC	Removed noise inject and heater funct.
04	2003-03-26	WKC	New part designations - entire chassis
03	2003-02-21	WKC	Added sw. positions 5&6
02	1999-04-29	JEE	Added 9-pin Amphen connector for noise control
01	1999-01-25	JEE	Cleaned up system supply pins

2000-01-05

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: OVERALL SCHEMATIC, Coax SW Cntl, SIS Meas Sys

File:

Design:

Schem Name: OVERALL SCHEMATIC

Drawn: jee 1998-11-23

Page: 1 of: 15

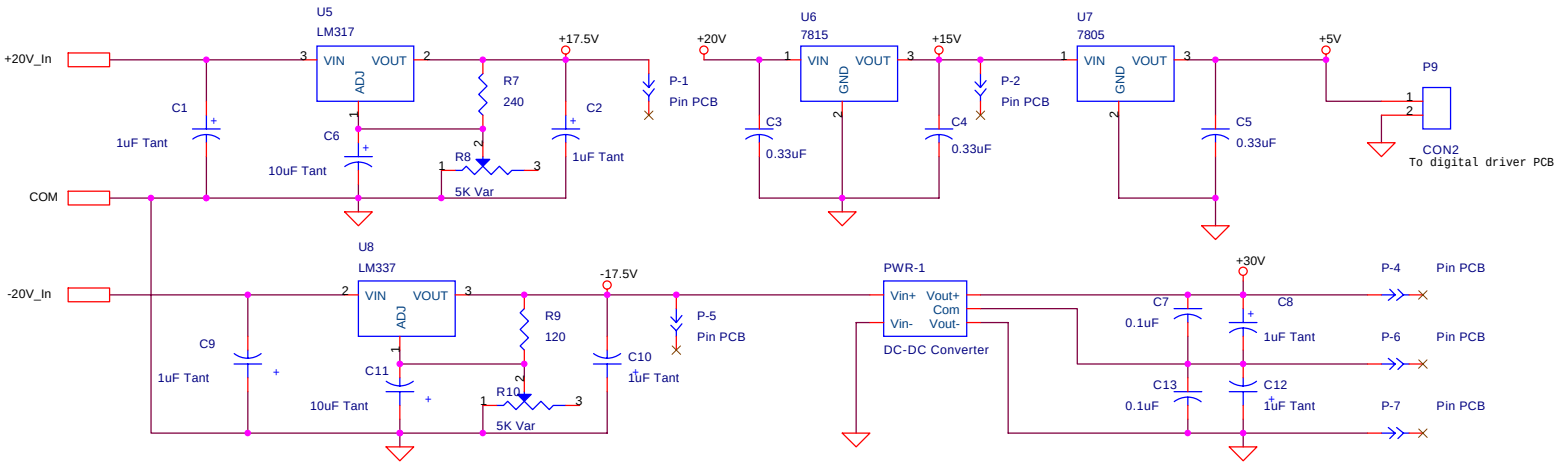
Dwg No: 04010700S004

Modified: 18:45:12 Friday, May 14, 2004

Size: A

Rev: 04

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN



Rev	Date	By	Description
08	2003-08-08	WKC	Removed noise diode circuitry
07	2003-03-26	WKC	New part designations - entire chassis
06	1999-08-04	JEE	Optisolator pins 3 & 4 swapped
05	1999-06-01	JEE	ISO1C control to active low
04	1999-04-29	JEE	Connections for IF switch
03	1999-03-25	JEE	Connected P-25 to remote pin on S-2
02	1999-02-23	JEE	Corrected Iso1A source to +20V
01	1999-01-25	JEE	Updated +20V pwr to +17.5V

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: Power Supply

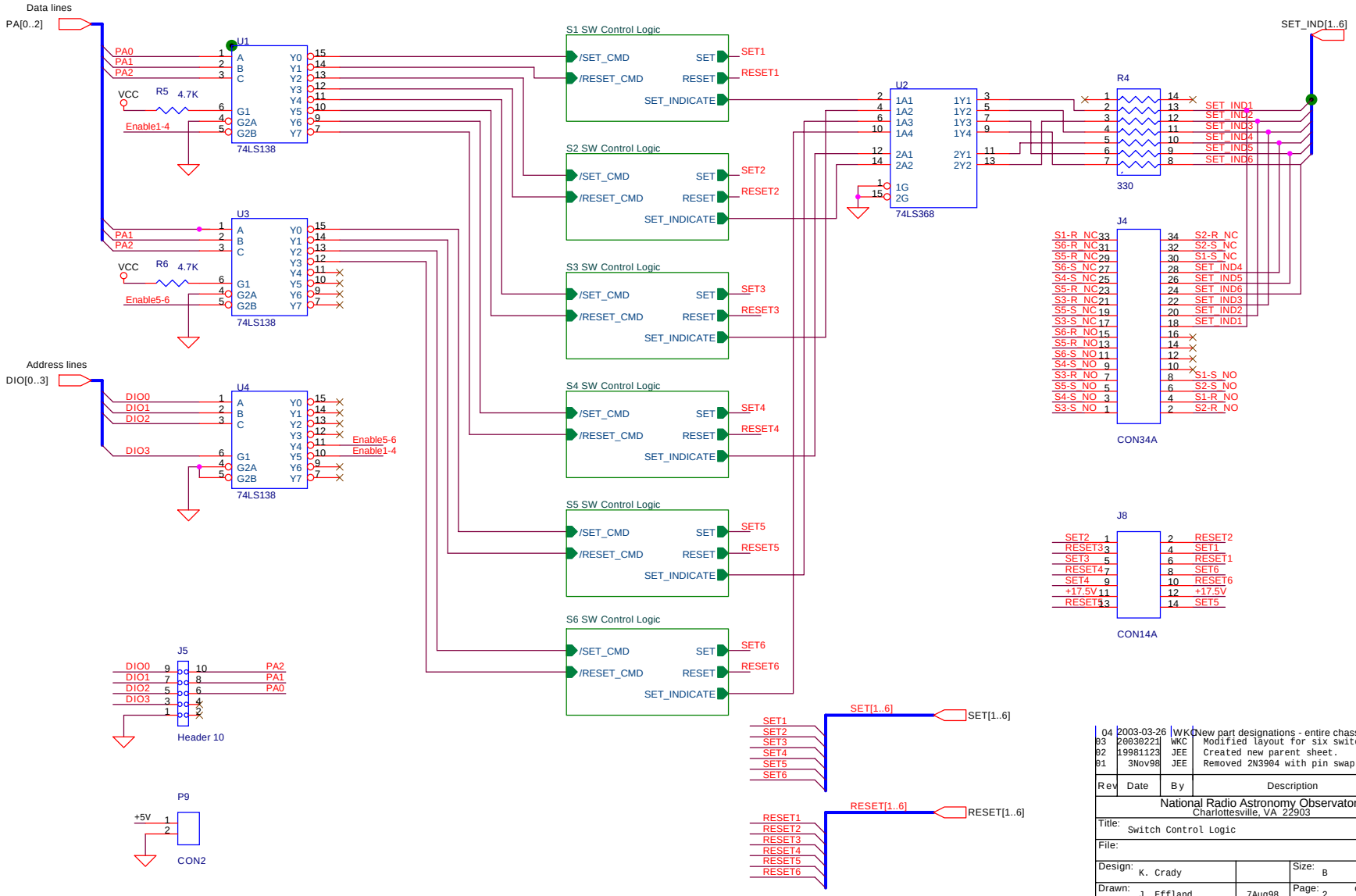
File:

Design: A.R. Kerr | 1984-01-13 | Size: B

Drawn: JEE | 1998-11-13 | Page: 3 of: 15

Dwg No: 04010700S004 | Rev: 07

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN



Rev	Date	By	Description
04	2003-03-26	WKC	New part designations - entire chassis
03	20030221	WKC	Modified layout for six switches
02	19981123	JEE	Created new parent sheet.
01	3Nov98	JEE	Removed 2N3904 with pin swap on 138's.

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: Switch Control Logic

File:

Design: K. Crady

Drawn: J. Effland 7Aug98

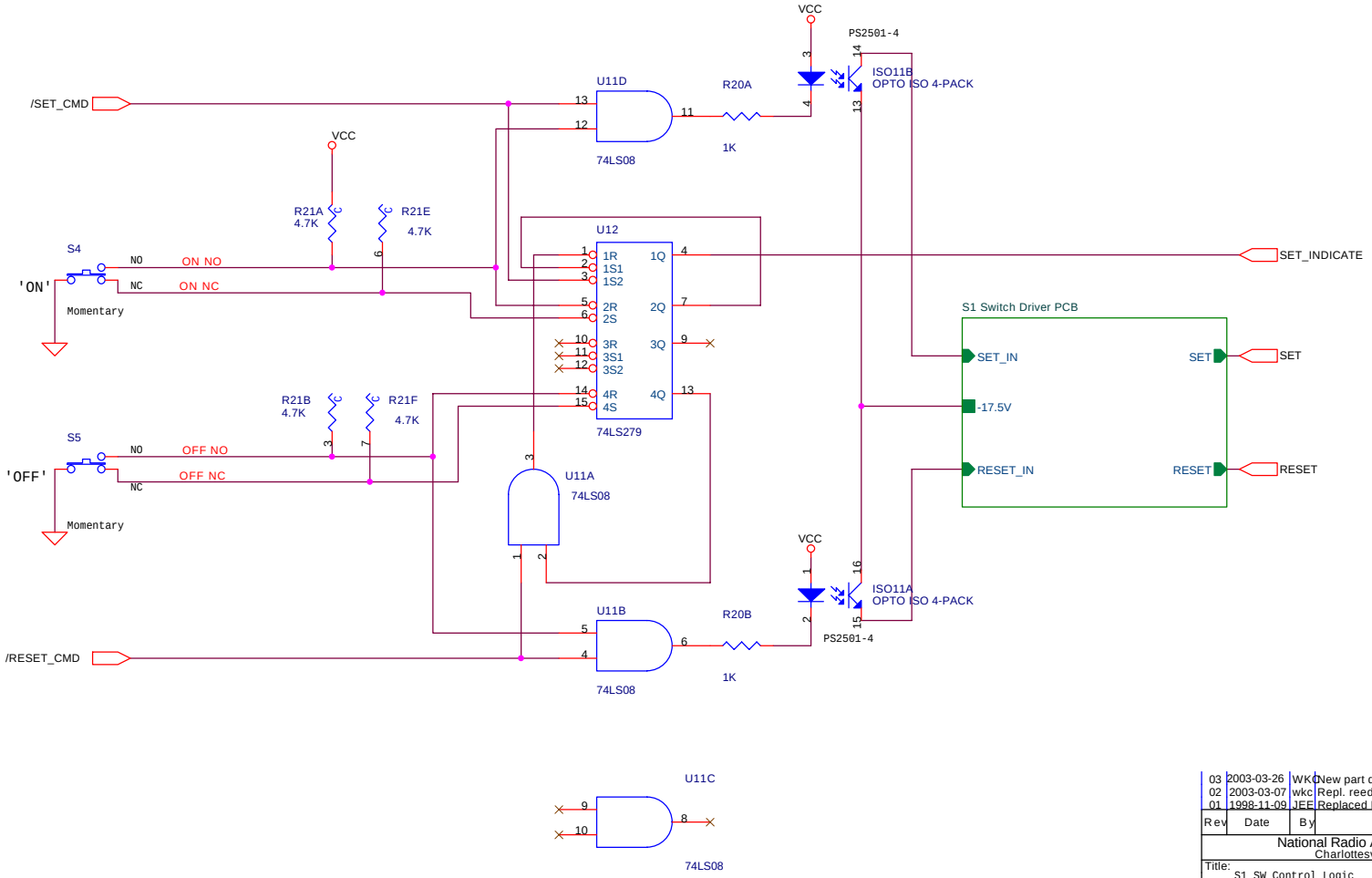
Size: B

Page: 2 of: 15

Dwg No: 04010700S004

Rev: 04

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN



Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
02	2003-03-07	wkc	Repl. reed relay w/opto-isolator ckt.
01	1998-11-09	JEF	Replaced LS00's with LS279

2000-01-05

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S1 SW Control Logic

File:

Design: K. Crady

Drawn: K. Crady

Schem Name: S1 SW Cntl Logic

Page: 4 of 15

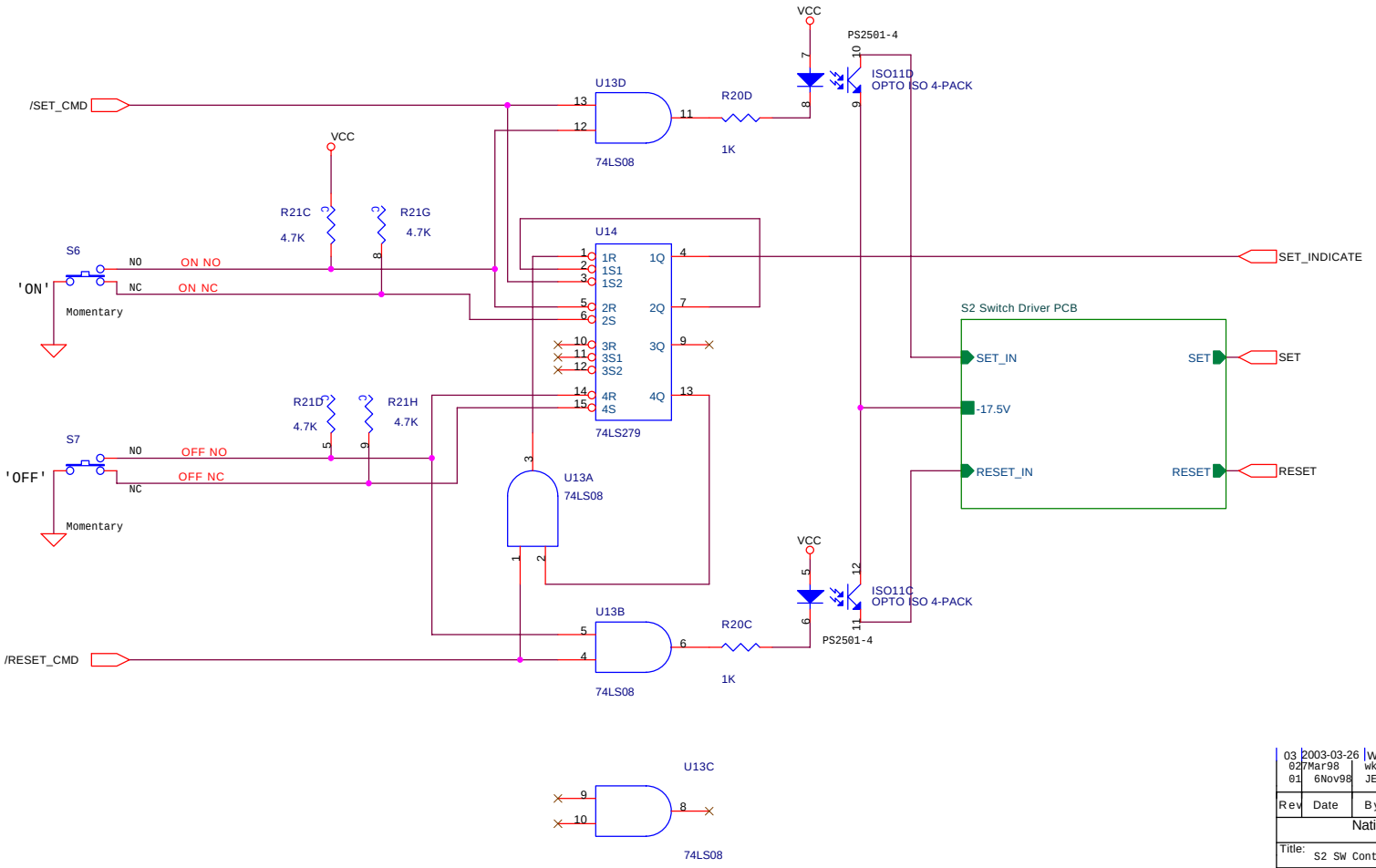
Dwg No: 04010700S004

Modified: 16:19:57 Wednesday, March 26, 2003

Size: B

Rev: 03

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN

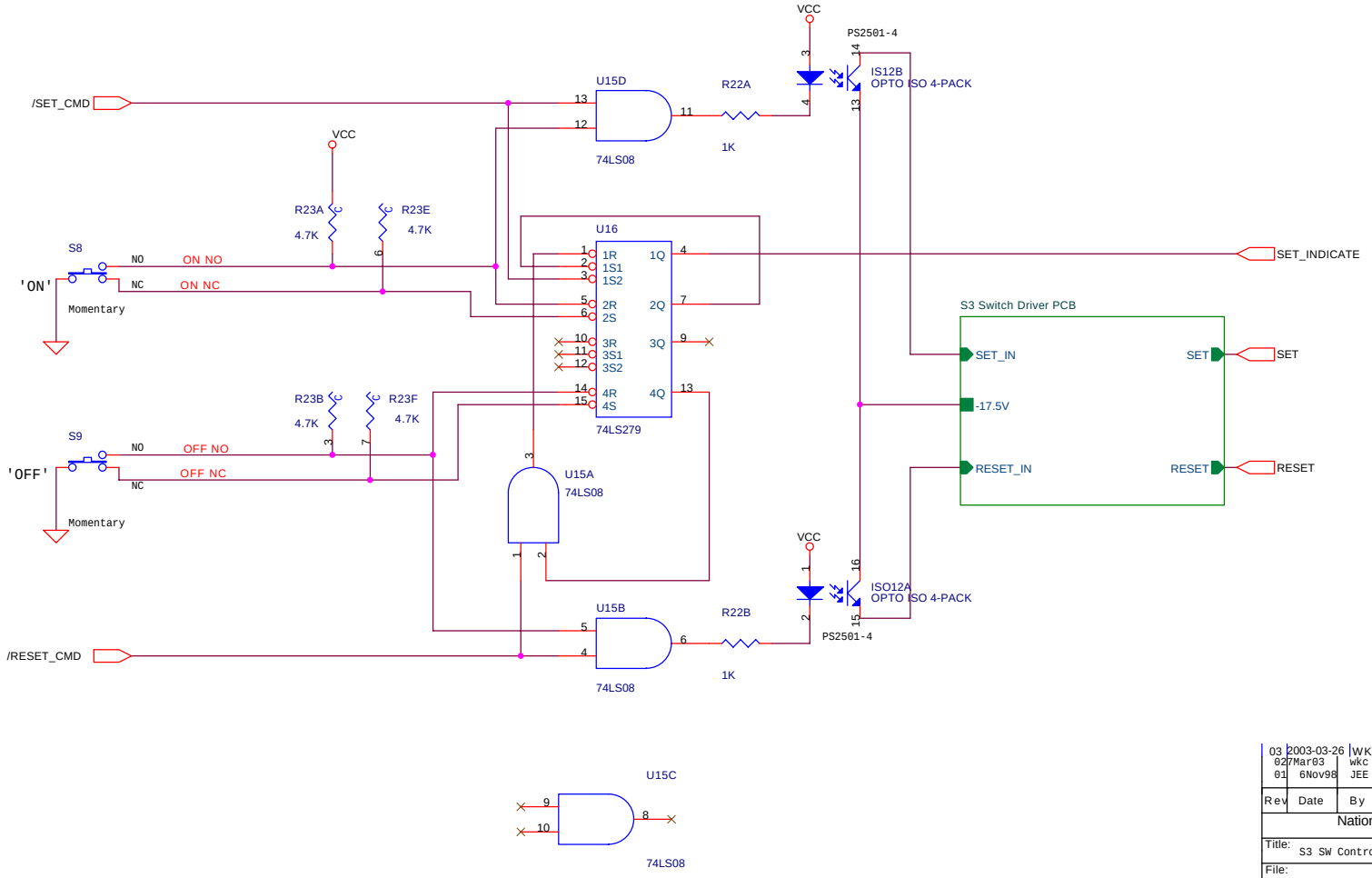


Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
02	7Mar98	wkc	Repl. reed relay w/opto-isolator ckt.
01	6Nov98	JEE	Replaced LS00's with LS279

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S2 SW Control Logic			
File:			
Design: K. Crady		Size: B	
Drawn: K. Crady		Page: 5 of: 15	
Dwg No: 04010700S004			Rev: 03

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN

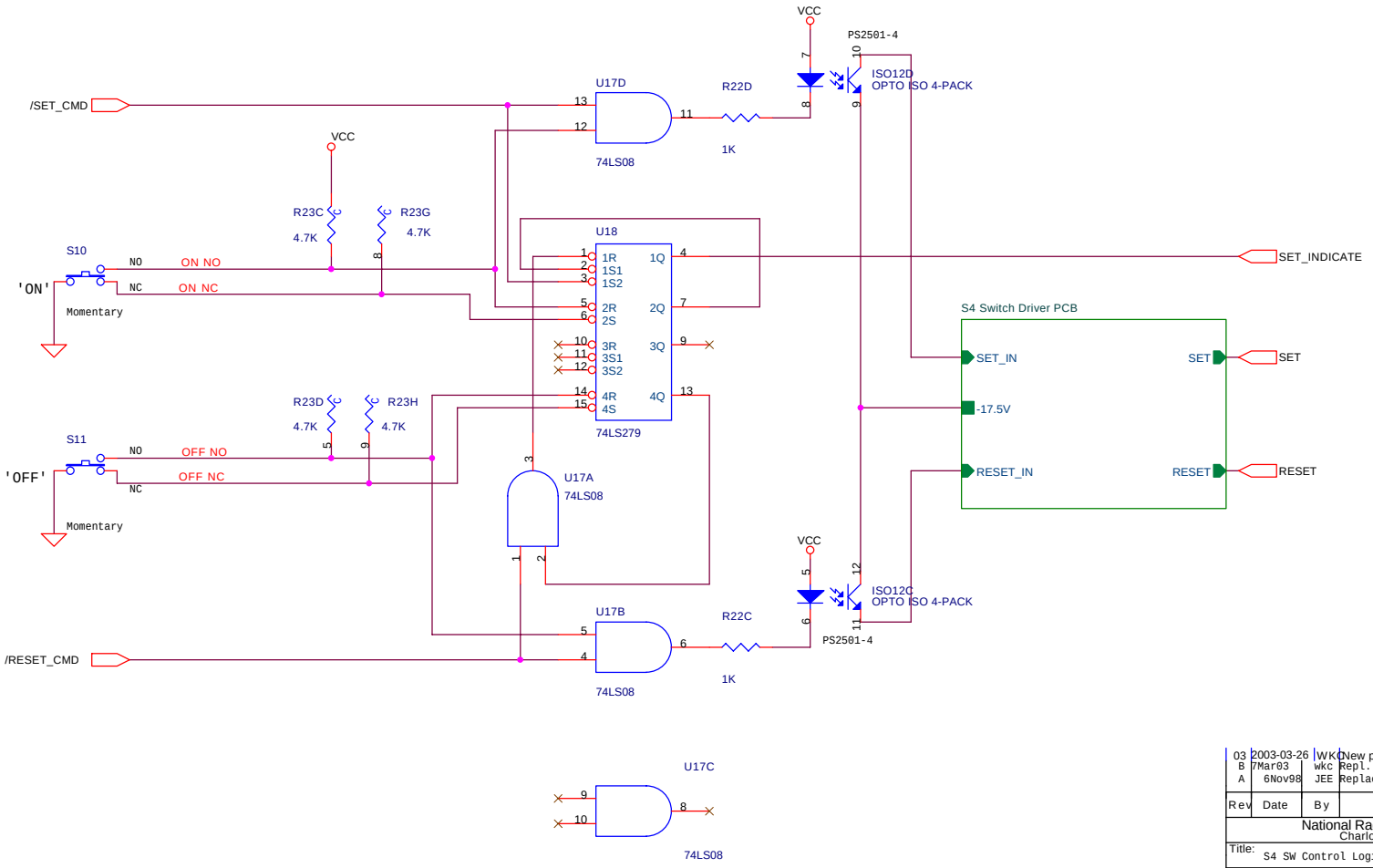


Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
02	7Mar03	wkc	Repl. reed relay w/opto-isolator ckt.
01	6Nov98	JEE	Replaced LS00's with LS279

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S3 SW Control Logic			
File:			
Design: K. Crady		Size: B	
Drawn: K. Crady		Page: 6 of: 15	
Dwg No: 04010700S004			Rev: 03

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN

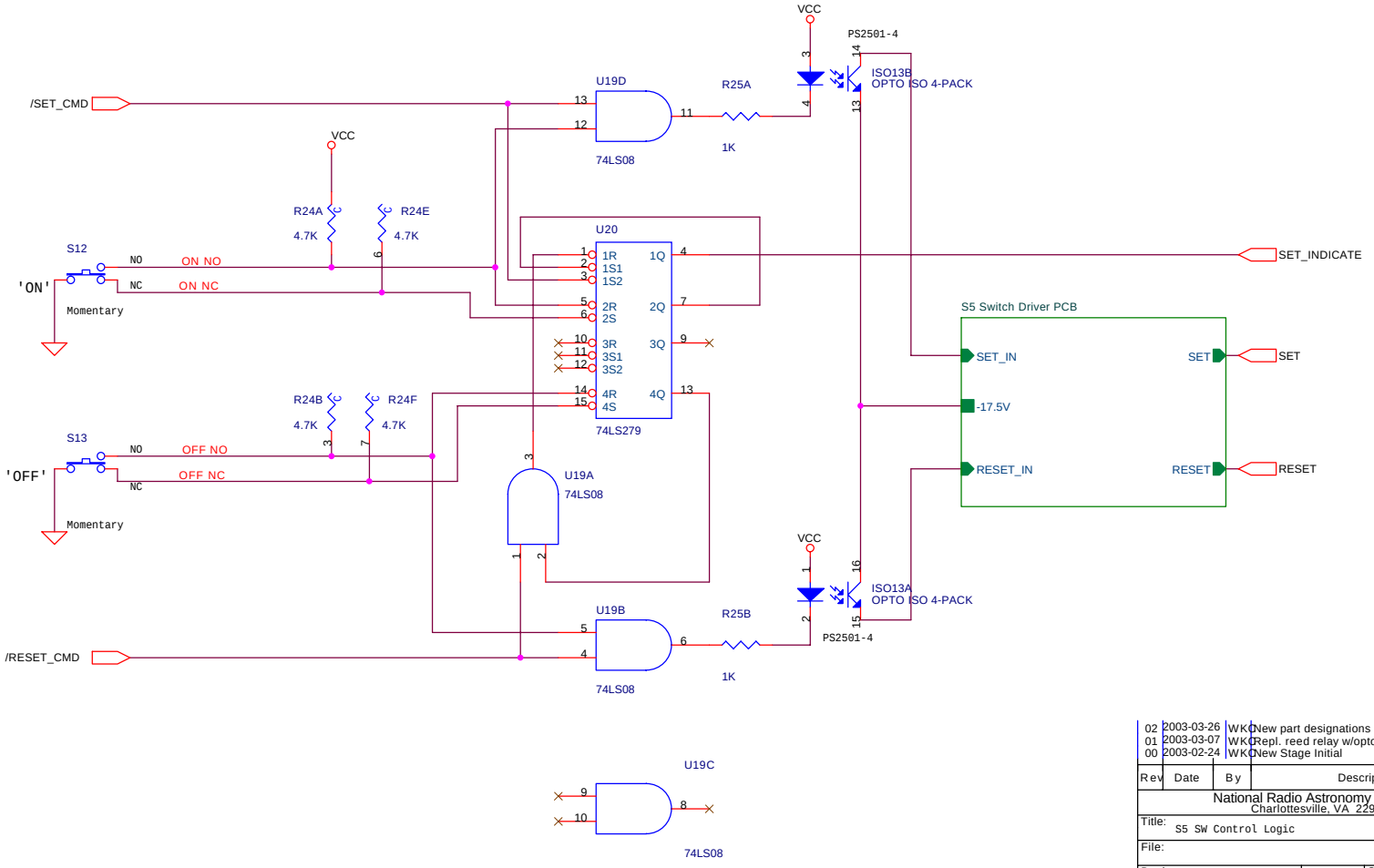


\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN

Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
B	7Mar03	wkc	Repl. reed relay w/opto-isolator ckt.
A	6Nov98	JEE	Replaced LS00's with LS279

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S4 SW Control Logic			
File:			
Design: K. Crady		Size: B	
Drawn: K. Crady		Page: 7 of: 15	
Dwg No: 04010700S004			Rev: 03



Rev	Date	By	Description
02	2003-03-26	WKC	New part designations - entire chassis
01	2003-03-07	WKC	Repl. reed relay w/opto-isolator ckt.
00	2003-02-24	WKC	New Stage Initial

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S5 SW Control Logic

File:

Design: WKC

Size: B

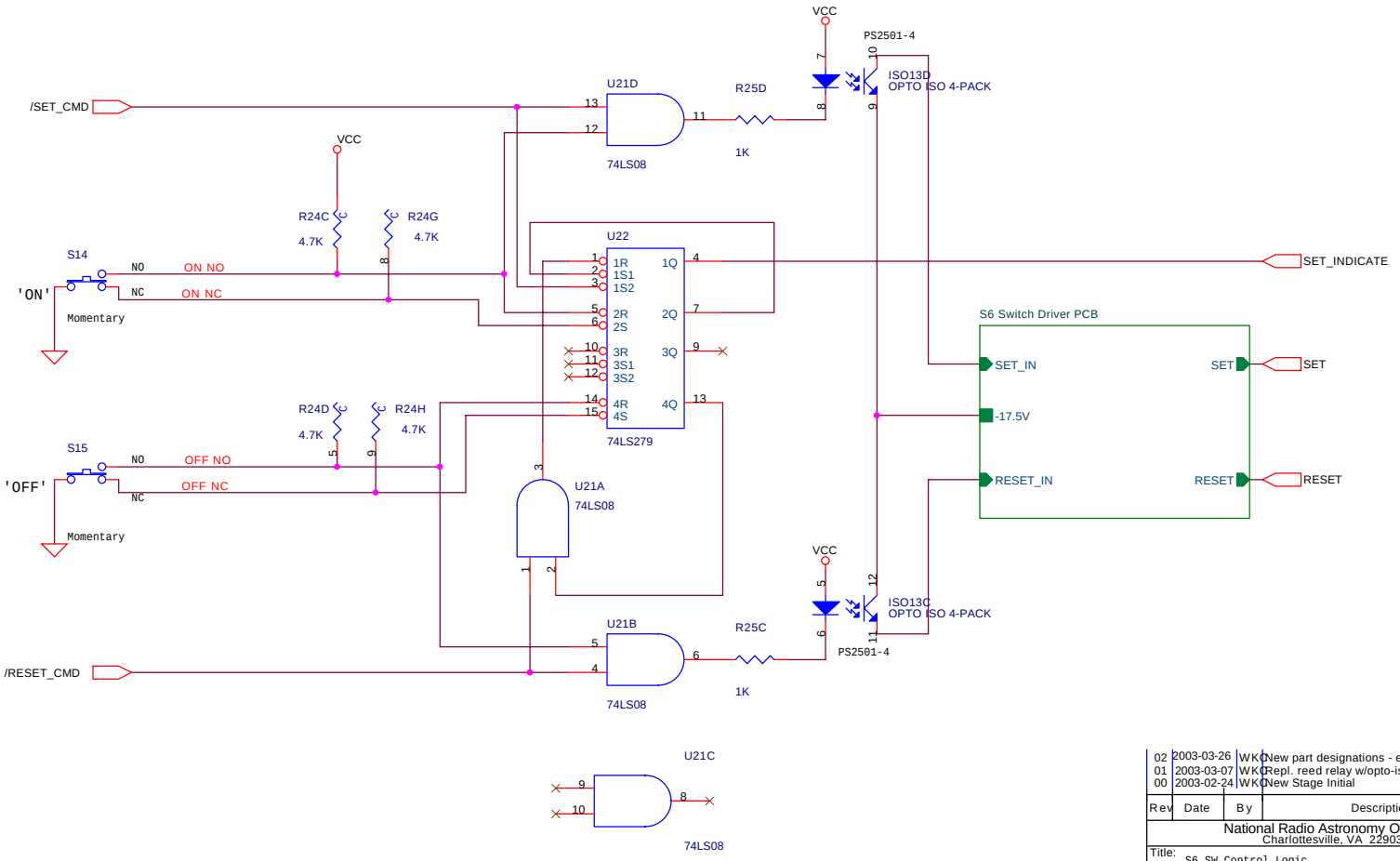
Drawn: WKC

Page: 8 of: 15

Dwg No: 04010700S004

Rev: 02

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN



Rev	Date	By	Description
02	2003-03-26	WKC	New part designations - entire chassis
01	2003-03-07	WKC	Repl. reed relay w/opto-isolator ckt.
00	2003-02-24	WKC	New Stage Initial

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S6 SW Control Logic

File: \\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN

Design: WKC

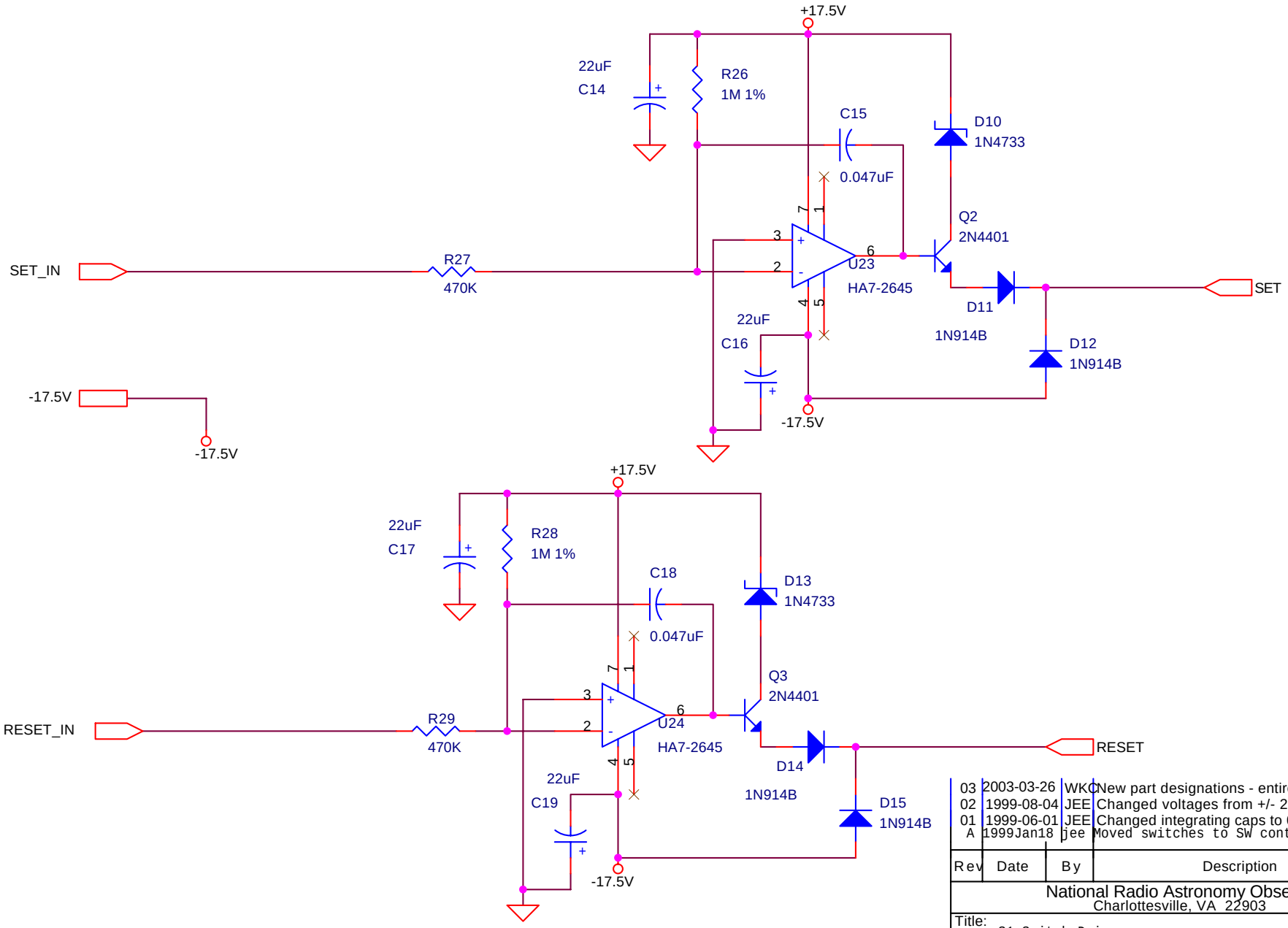
Drawn: WKC

Size: B

Page: 9 of: 15

Dwg No: 04010700S004

Rev: 02



Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
02	1999-08-04	JEE	Changed voltages from +/- 20 to 17.5V
01	1999-06-01	JEE	Changed integrating caps to 0.047uF
A	1999Jan18	jee	Moved switches to SW control logic sheet

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S1 Switch Driver

File:

Design: A.R. Kerr

Drawn: Jee 11Nov98

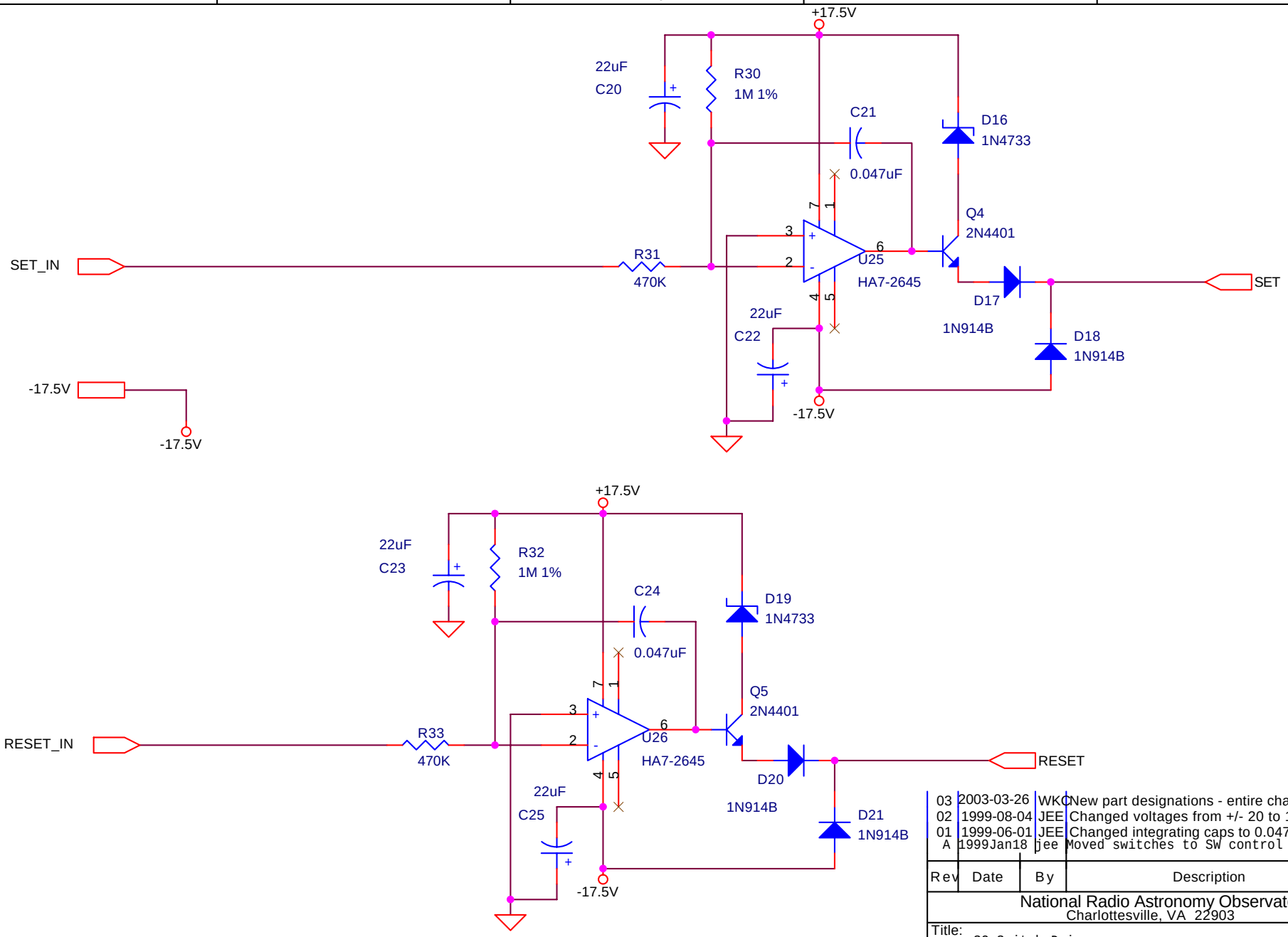
Size: A

Page: 10 of: 15

Dwg No: 04010700S004

Rev: 03

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN



Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
02	1999-08-04	JEE	Changed voltages from +/- 20 to 17.5V
01	1999-06-01	JEE	Changed integrating caps to 0.047uF
A	1999Jan18	jee	Moved switches to SW control logic sheet

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S2 Switch Driver

File:

Design: A.R. Kerr

Size: A

Drawn: Jee

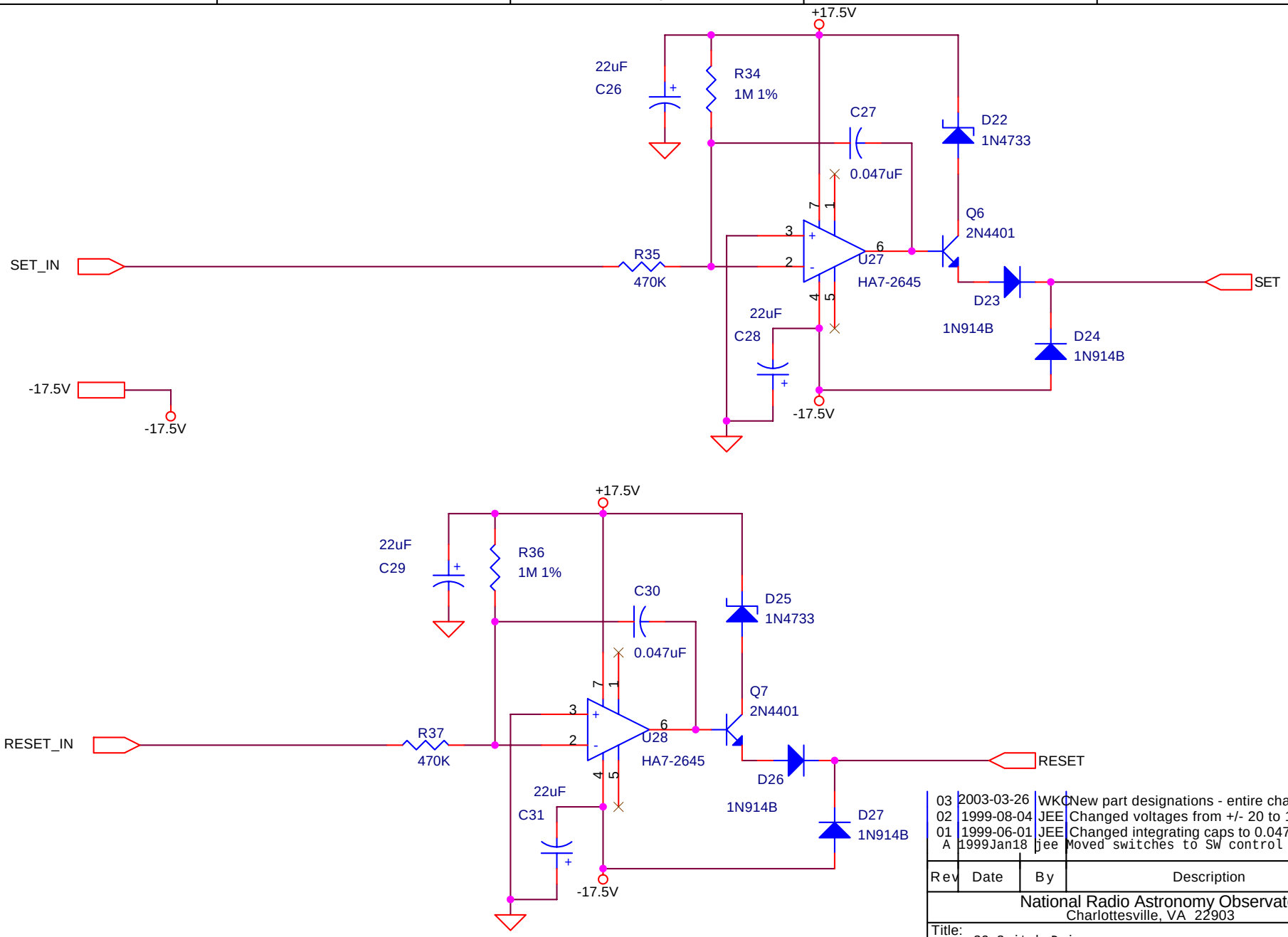
11Nov98

Page: 11 of: 15

Dwg No: 04010700S004

Rev: 03

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN



Rev	Date	By	Description
03	2003-03-26	WKC	New part designations - entire chassis
02	1999-08-04	JEE	Changed voltages from +/- 20 to 17.5V
01	1999-06-01	JEE	Changed integrating caps to 0.047uF
A	1999Jan18	jee	Moved switches to SW control logic sheet

National Radio Astronomy Observatory
Charlottesville, VA 22903

Title: S3 Switch Driver

File:

Design: A.R. Kerr

Drawn: Jee 11Nov98

Size: A

Page: 12 of: 15

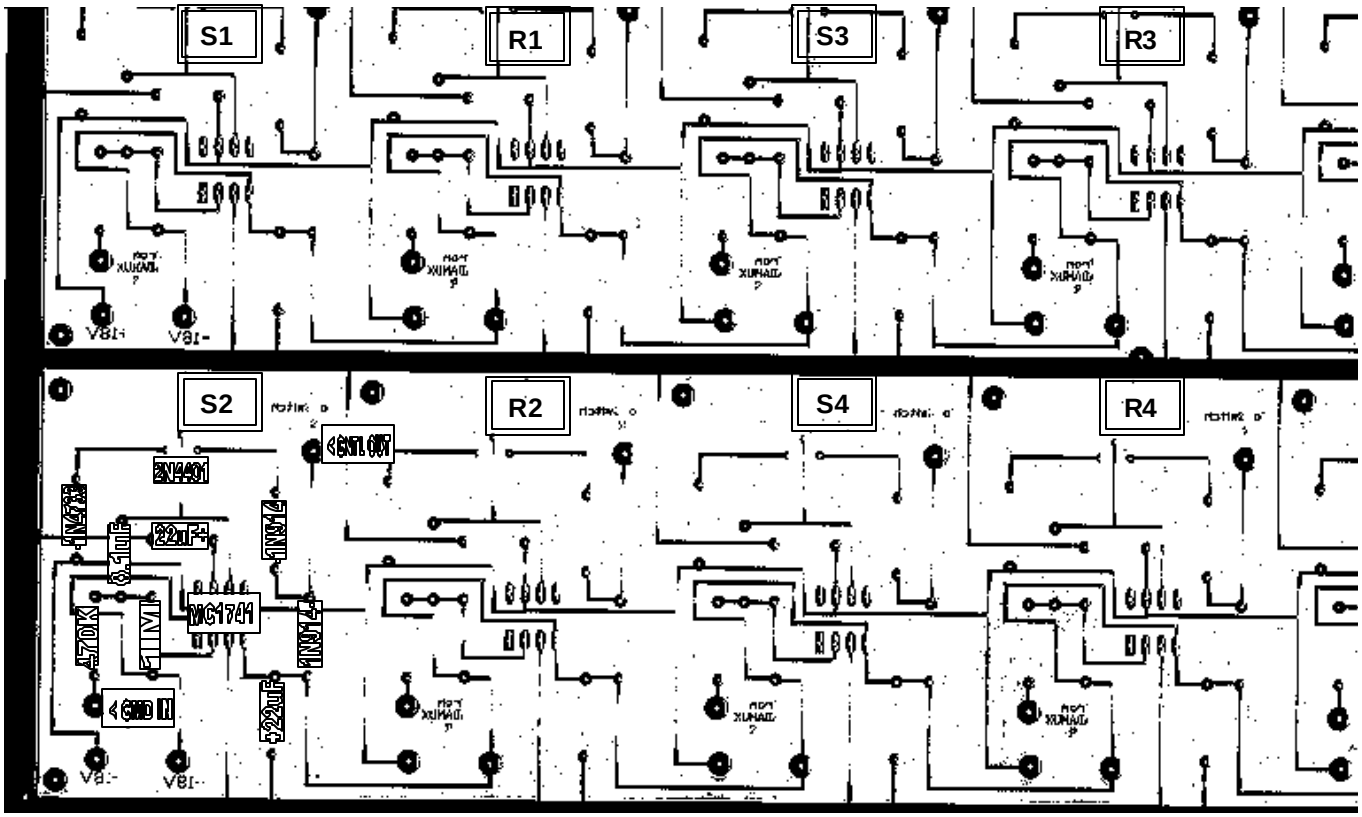
Dwg No: 04010700S004

Rev: 03

\\CVFILER\CV-CDL-SIS\DOCS\RACK\COAX SWITCH DRIVER\REVISED LAYOUT 2003\417S004.REVISED.DSN

Attachment 2: Switch Control PCB Layout

Attachment 3: Switch Driver PCB Layout



Attachment 4: Power Supply PCB Layout