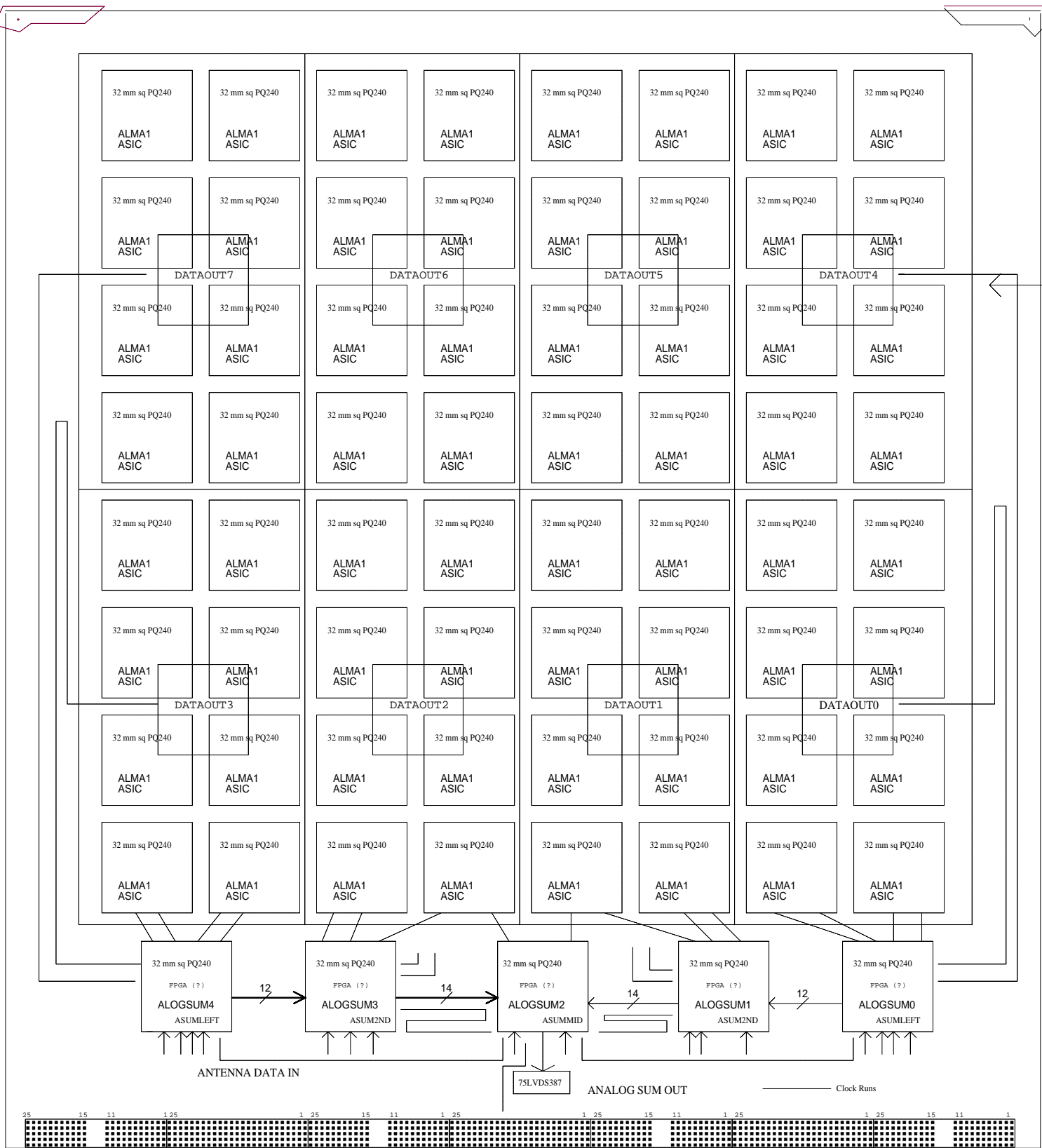
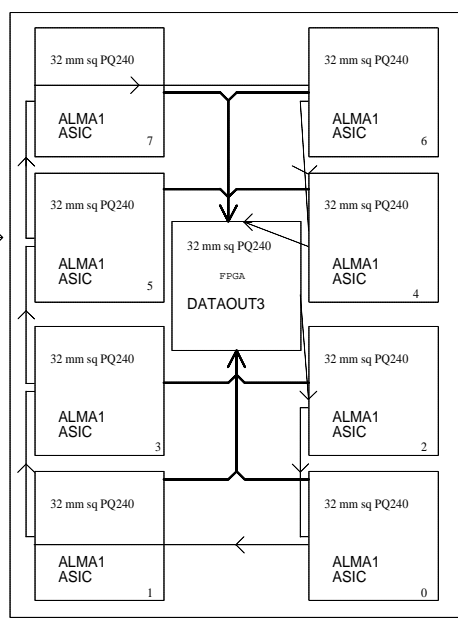


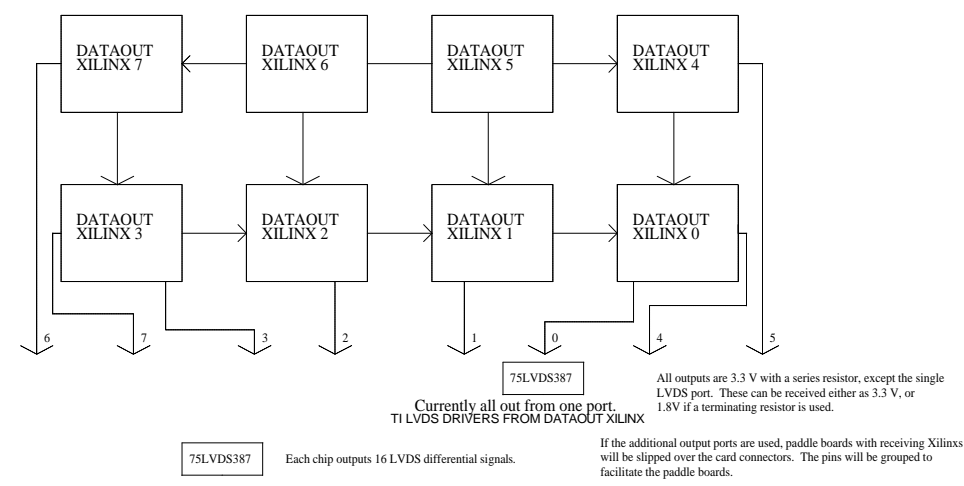
400 mm deep  
15.7 inches



Each DATAOUT Xilinx is connected to eight ASICs, on the opposite side of the card, via two tri-state busses, as shown.

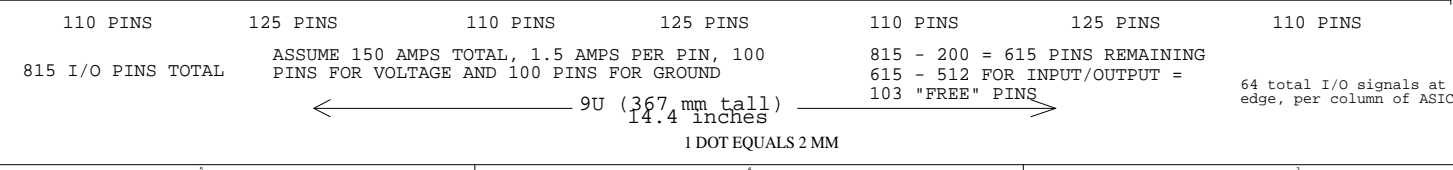


Dataout Xilinx on Back of Card



There will be 8, 16 bit output busses. At 125 MHz, these can drain the card in less than 1 ms. The current LTA will use a single 8 bit differential LVDS bus, running at 125 MHz.

There are 2 bits from each of 2 memory cards for each of 4 ants, and both the MAIN and AUX sets of ants = 2x2x4x2=32 input signals per column of ASICs.



OUTPUTS  
2 BUS OF 16 BIT LVDS DIFFERENTIAL DATA 2\*16\*2=64 PINS  
7, 16 Bit Output data busses = 112 PINS  
16 BIT DATA INPUT = 256 PINS

INPUT/OUTPUT = 432 PINS

In j:/orcad/hwdwgs/corr card/figures.opj as 8x8 240PQFP

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