centerbus\[1:0\] is a two bit field in the program word. It selects the centerbus driver source 0, 1, 2, or 3.

DL stands for Data Left

DBR stands for Data Bottom Right

DTR stands for Data Top Right

DBR\[15:0\]

DTR\[15:0\]

DBR

DTR

DBR\[15:0\]

DTR\[15:0\]

Data path 1

Data path 2

Data path 3

Data path 4

Figure 3

Chip 125 MHz Data Input/Output
Where Rx represents Row number as defined in Figure 2.

For the remaining 12 blocks of 256 Lags:

1) Two 2-bit data input signals from vertical axis
2) Two 2-bit data input signals from horizontal axis
3) Two 2-bit data output signals on vertical axis
4) Two 2-bit data output signals on horizontal axis
5) 2-bit data input signals from last block
6) 16-bit output results bus
7) 16-bit input results bus
8) 2-bit results bus select bits (SEL[1:0])
9) Two 2-bit data output signals on horizontal axis
10) Two 2-bit data output signals on vertical axis
11) 16-bit accumulator reset
12) 16-bit output results bus
13) Delayed blanking
14) Seq. dump to storage
15) DUMP enable
16) 125 MHz clock
17) 64-stage shift register
18) 64-LAG correlator 0
19) 64-LAG correlator 1
20) 64-LAG correlator 2
21) 64-LAG correlator 3
22) CONCAT = R0-M15 * R0-M14
23) CONCAT = R0-M11 * R0-M10
24) CONCAT = R0-M7 * R0-M6
25) CONCAT = WRAP-BLK0

For Block 5:
- LEAD-BLK = 1
- LEAD-CTRL[1:0] = 0 0

For Block 0:
- LEAD-BLK = 0
- LEAD-CTRL[1:0] = 0 1

For Block 15:
- LEAD-BLK = 1
- LEAD-CTRL[1:0] = 1 0

For Block 10:
- LEAD-BLK = 0
- LEAD-CTRL[1:0] = 1 1

When the chip is on a diagonal, the self products on the chip diagonals have LEAD-BLK = 0. This means there is no extra delay stage inserted.

For Block 4:
- LEAD-BLK = 0
- LEAD-CTRL[1:0] = 1 0

Similarily, OVERSAMP = RxOVERSAMP = 1 in all presently planned operating modes.
[Diagram and text from page]
**FIGURE 6**

**ONE CORRELATOR LAG**

1/5/00

---

**5-BIT ACCUMULATOR**

**2-BIT X 2-BIT MULTIPLIER**

(Use the BIASED MULTIPLICATION TABLE. See below.)

**4-BIT RIPPLE-THRU PRE-SCALER**

(Asynchronous Reset)

**5-BIT ADDER**

**GATED 125 MHz CLOCK**

**GATED BY BLANKING**

**MS BIT P-INPUT**

**LS BIT P-INPUT**

**P-INPUT**

01 00 11 10

**D-INPUT**

01 9 3 -3 -9
00 3 1 -1 -3
11 -3 -1 1 3
10 -9 -3 3 9

**UNBIASED MULTIPLICATION TABLE**

**BIASED MULTIPLICATION TABLE**

Add 9, then divide by 2

---

**FULLACC=1 SPECIFIES A 25 BIT INSTEAD OF A 21 BIT ACCUMULATOR.**

FULLACC defined on Figure 4 for the 256 Lag Block.

---

**FULLACC=1 SPECIFIES A 25 BIT INSTEAD OF A 21 BIT ACCUMULATOR.**

FULLACC defined on Figure 4 for the 256 Lag Block.

---

**MS  LS  WEIGHT**

<table>
<thead>
<tr>
<th>MS</th>
<th>LS</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>+3</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>+1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>-3</td>
</tr>
</tbody>
</table>

---

This provides an Asynchronous Jam Load

---

A synchronous dump to storage could be used if desirable.
FIGURE 7
CHIP RESULTS OUTPUT BUS

RESULTS READ-OUT

1) A 4-Bit BLOCK input from the sequencer selects one of the 16, 256 lag, baseline correlator blocks for read-out.

2) A 2-bit SUBBLOCK input from the sequencer selects one of the four 64 lag sub-block correlators for read-out.

3) READCLK shifts out the 16 bit wide bus. The 64 lag sub-block to be shifted out is selected by the SEL[0..5] field. The chip must be output enabled via XOE and YOE.

RESULTS LSB, 256 LAG BLOCK 0
RESULTS LSB, 256 LAG BLOCK 1
RESULTS LSB, 256 LAG BLOCK 2
RESULTS LSB, 256 LAG BLOCK 3
RESULTS LSB, 256 LAG BLOCK 4
RESULTS LSB, 256 LAG BLOCK 5
RESULTS LSB, 256 LAG BLOCK 6
RESULTS LSB, 256 LAG BLOCK 7
RESULTS LSB, 256 LAG BLOCK 8
RESULTS LSB, 256 LAG BLOCK 9
RESULTS LSB, 256 LAG BLOCK 10
RESULTS LSB, 256 LAG BLOCK 11
RESULTS LSB, 256 LAG BLOCK 12
RESULTS LSB, 256 LAG BLOCK 13
RESULTS LSB, 256 LAG BLOCK 14
RESULTS LSB, 256 LAG BLOCK 15

RESULTS MSB, 256 LAG BLOCK 0
RESULTS MSB, 256 LAG BLOCK 1
RESULTS MSB, 256 LAG BLOCK 2
RESULTS MSB, 256 LAG BLOCK 3
RESULTS MSB, 256 LAG BLOCK 4
RESULTS MSB, 256 LAG BLOCK 5
RESULTS MSB, 256 LAG BLOCK 6
RESULTS MSB, 256 LAG BLOCK 7
RESULTS MSB, 256 LAG BLOCK 8
RESULTS MSB, 256 LAG BLOCK 9
RESULTS MSB, 256 LAG BLOCK 10
RESULTS MSB, 256 LAG BLOCK 11
RESULTS MSB, 256 LAG BLOCK 12
RESULTS MSB, 256 LAG BLOCK 13
RESULTS MSB, 256 LAG BLOCK 14
RESULTS MSB, 256 LAG BLOCK 15

16-BIT RESULTS BUSES
FROM 16 LAG BLOCKS
FROM FIGURE 4

2-BIT CORR
SELECT
SUB-BLOCK
4-BIT CORR
BLOCK SELECT
SHIFT-OUT
CONTROL LOGIC

1 to 48
DEMUX

A sequencer on the correlator card generates X-Axis and Y-Axis enable signals to output enable a single correlator chip onto the correlator card results output bus. Alternately the XOE and YOE pins could be tied together on the card, and driven from a single select line. Have the pins adjacent to each other.

The above logic is repeated with: DIAGONAL BLOCK5 decoded, and DIAGONAL5AUTO used. This outputs SHIFT OUT CLOCK 20, 21, 22, and 23.

The above logic is repeated with: DIAGONAL BLOCK10 decoded, and DIAGONAL10AUTO used. This outputs SHIFT OUT CLOCK 40, 41, 42, and 43.

The above logic is repeated with: DIAGONAL BLOCK15 decoded, and DIAGONAL15AUTO used. This outputs SHIFT OUT CLOCK 60, 61, 62, and 63.
The delay line above is also shown on Figure 1 in the blanking signal line.
NOTE: SEVERAL OPERATING MODES ARE POSSIBLE BY PROGRAMMING THE CORRELATOR CHIPS.

AUX BUS: Inputs going to the two chips on either side of the bus are not shown for clarity.

Each data bus has 4 antennas x 2 memory cards x 2 bits = 16 lines. 16 lines x 2 lines per chip x 8 chips = 256 input pins required.

FIGURE 10
ALMA CORRELATOR CARD.

NOTE: SEVERAL OPERATING MODES ARE POSSIBLE BY PROGRAMMING THE CORRELATOR CHIPS.

The modes shown are:

- **T0 0**: Antennas 29, 29, and 31
- **T1 0**: Antennas 60, 61, 62, and 63
- **T2 1**: Antennas 28, 29, 30, and 31
- **T4 3**: Antennas 32, 33, 34, and 35

The mode is determined by the programming of the correlator cards.

INPUT/OUTPUT PINS

NOTE: SEVERAL OPERATING MODES ARE POSSIBLE BY PROGRAMMING THE CORRELATOR CHIPS.

Each data bus has 4 antennas x 2 memory cards x 2 bits = 16 lines. 16 lines x 2 lines per chip x 8 chips = 256 input pins required.

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NOTE: SEVERAL OPERATING MODES ARE POSSIBLE BY PROGRAMMING THE CORRELATOR CHIPS.

Each data bus has 4 antennas x 2 memory cards x 2 bits = 16 lines. 16 lines x 2 lines per chip x 8 chips = 256 input pins required.
64 ANTENNAS
2 CHANNELS
2 BITS

32 8-SIGNAL CABLES
ON MOTHERBOARD

CAPTURE F/Fs
CLOCK RATE 125 MHz

ANTENNA 0 THRU 31
ANTENNA 32 THRU 63

CARD MAIN BUS
CARD AUX BUS

V X H = 0-31 X 0-31
V X H = 0-31 X 32-63
V X H = 32-63 X 0-31
V X H = 32-63 X 32-63

H connected to V
inside the chip.

V and H refer to the Vertical and Horizontal Axes within the chips, as defined in Figure 2.

The above drawing represents which signals are routed to which cards. The actual method of distributing the signals to the cards is to be determined.

FIGURE 9
12/15/99
SIGNAL DISTRIBUTION TO SET OF FOUR CORRELATOR CARDS
BREAK-DOWN OF 64 X 64 ANTENNA CROSS MULTIPLIER PLANE INTO 4 PRINTED CIRCUIT CARDS

CROSS MULTIPLIER PLANE
(AUTO-CORRELATORS ON MATRIX DIAGONAL)
Each data bus has 4 antenna * 2 memory cards, 16 lines x 2 lines per chip x 8 chips = 256 input pins required.

Required modes:

- **T1 0**
- **T3 2**
- **T5 3**
- **T0 0**
- **T7 3**

Note: Several operating modes are possible by programming the correlator chips. This mode is also used on the self product card.

**INPUT/OUTPUT PINS**

Wire all AUX BUS signals, even though they may not be used. Signals off the top and sides of the bus are test points. These can be enabled by appropriate setting of the bits in the program words. The left test points would require grounding the pull-up resistor into the LTOR-IN.
All data paths are two bits wide.
FIGURE 12
TIMING DIAGRAMS

All signals are initially shown after the buffer register of the input pin. Blanking is shown 12 clocks long for convenience. Actually it will be longer duration.

BLANKING
C125

DELAYED BLANKING
12 Clocks long

GATED CLOCK
12 Clocks Missed

PRIME THE SHIFT REGISTER
During blanking, the shift register is primed with data.

SEQ PULSE

SEQ DUMP TO STORAGE