TDC-GPX

Ultra-high Performance 8 Channel
Time-to-Digital Converter

Datasheet

MAY 31ST , 2006

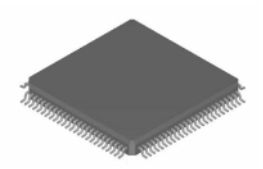
acam - solutions in time

Precision Time Interval Measurement

acam
mess-electronic

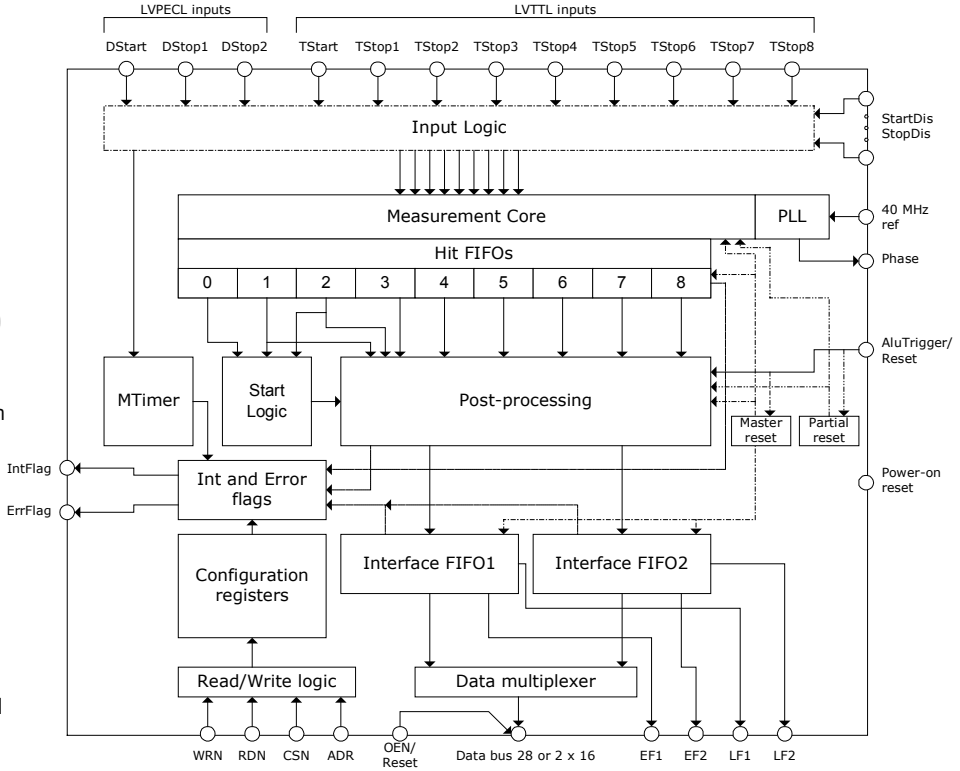
1. Introduction

1.1 System overview



TQFP100

TFBGA120



I-Mode

- 8 channels with typ. 81 ps resolution
- 9 LVTTL inputs, optional 3 LVPECL inputs
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range 9,8 µs, endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip

G-Mode

- 2 channels with 40 ps resolution
- Differential LVPECL inputs, optional LVTTL
- Measurement range 0 ns to 65 µs
- 5.5 ns pulse-pair resolution between edges of equal slope with 32-fold multi-hit = 182 MHz peak rate
- Minimum pulse width 1.5 ns
- Trigger to rising **and** falling edge
- Optional Quiet Mode (no ALU operation and Data-output during measurements)
- 20 MHz continuous rate per channel
- 40 MHz continuous rate per chip

R-Mode

- 2 channels with 27 ps resolution
- Differential LVPECL inputs, optional LVTTL
- Measurement range 0 µs up to 40 µs
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Optional Quiet Mode (no ALU operation and Data-output during measurements)
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

M-Mode

- 2 channels with 10 ps resolution (70 ps peak-peak)
- Differential LVPECL inputs
- Measurement range 0 ns up to 10 µs
- Single hit per Start and channel
- Trigger to rising or falling edge
- Quiet Mode (no ALU operation and Data-output during measurements)
- Max. 500 kHz continuous rate per channel
- Max. 1 MHz continuous rate per chip

General

- Start retrigger option (besides M-Mode)
- Packages: TQFP100, TFBGA120
- IO voltage 3.0 V – 3.6 V
- Core voltage 2.3 V – 3.6 V regulated by resolution adjust unit
- Data bus: 28 Bit or 2 x 16 Bit asynchronous with Chipselect, Readstrobe, Writestrobe
- 40 MHz continuous rate per chip
- Address range: 4 Bit

1.2 Index

1.3 Electrical Characteristics

Absolute Maximum Ratings (Vss = 0V, Tj = 25°C)

Parameter		Symbol	Condition	Rated Value	Unit
Supply voltage	I/O	Vddo		-0.3~+3.6	V
	Core	Vddc	Vdcc < Vddo + 0.6V	-0.3~+3.6	
	Hardmacro	Vddc-h	Vdcc < Vddo + 0.6V	-0.3~+3.6	
	Oscillator	Vddc-o	Vdcc < Vddo + 0.6V	-0.3~+3.6	
	Diff. inputs	Vdde		-0.3~+3.6	
Input voltage	5V Tolerant Buffers	Vi	Vddo = +0.3~3.6V	-0.3~6.0	V
Output current	1 mA Buffer	Io	-	-5~+5	mA
	4 mA Buffer			-9~+9	
Storage temperature		Tstg		-65 to 150	°C
Junction temperature		Tj		-40 to 125	°C
Thermal resistance	junction-ambient	R_{thj-a}	TQFP100	96	K/W
			TFBGA120	105	

Terminal Capacitance

Terminal	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Input	Ci	measured @Vdd = Vi = Vo = Vss, f = 1 MHz, Ta = 25°C	-	6	-	pF
Output	Co		-	9	-	
Bidirectional	Cio		-	10	-	

DC Characteristics (Vddo = 3.3 V ± 0.3 V, Vss = 0 V, Tj = -40 to +85°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
High-level input voltage	Vih	TTL 5V tolerant input	2.0	-	5.5	V
Low-level input voltage	Vil	TTL 5V tolerant input	0.0	-	0.8	
High-level output voltage	Voh		2.4			
Low-level output voltage	Vol				0.4	
Supply current			Typ			mA
	Vddo	I/O	1.4 + Bus			
	Vddc	Core	20			
	Vddc-h	Hardmacro	7			
	Vddc-o	Oscillator	4			
	Vdde	Diff. inputs	19			

LVPECL inputs:

DC Parameters (VDD = 3.3 V±5 %, Tj = 0°C to 125°C)

Parameter	Val	Condition
VinOS	Vdde-1.53V < VinOS < Vdde-0.89V	-
VinDF	0.2V < VinDF < 2.1V	-

VinOS = Input offset voltage, (Via+Vian)/2
VinDF = Input differential voltage,
Via = Input voltage of A
Vian = Input voltage of AN

1.3.1 Bus Timings

(Vddo = Vddc = 3.3 V, Ta = +25°C)

Write operations

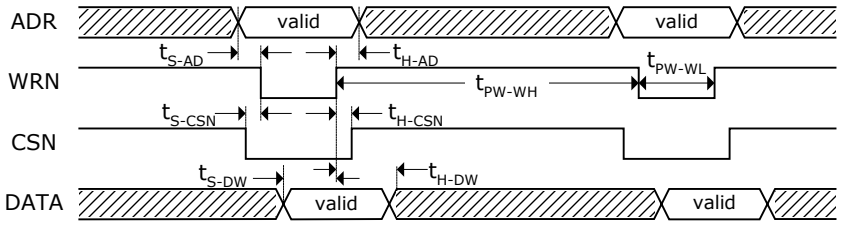


Figure 1

Spec	Description	Min (ns)	Max (ns)
t_{S-AD}	Address Setup Time	2	-
t_{H-AD}	Address Hold Time	0	-
t_{PW-WL}	Write LOW Time	6	-
t_{PW-WH}	Write HIGH Time	6	-
t_{S-DW}	Write Data Setup Time	5	-
t_{H-DW}	Write Data Hold Time	4	-
t_{S-CSN}	Chip Select Setup Time	0	-
t_{H-CSN}	Chip Select Hold Time	0	-

Read Operations

It is not allowed to read from an empty FIFO !

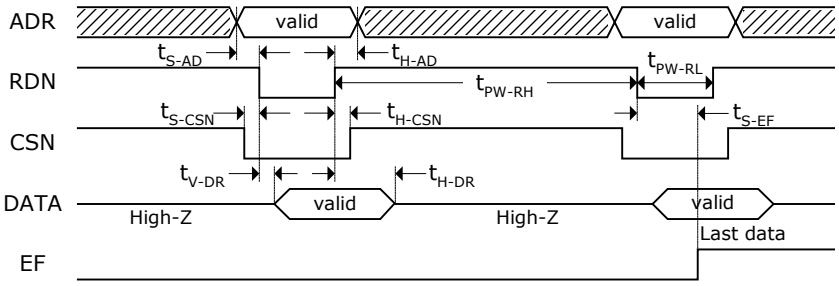


Figure 2

Spec	Description	Min (ns)	Max (ns)	
t_{S-AD}	Address Setup Time	2	-	* This value depends on the capacitive load and has to be confirmed by evaluation. This value also depends on the adjusted resolution. ** Can be prolonged infinitely with OEN = 0 (driving the bus permanently) and stable address.
t_{H-AD}	Address Hold Time	0	-	
t_{PW-RL}	Read LOW Time	6	-	
t_{PW-RH}	Read HIGH Time	6	-	
t_{V-DR}	Read Data Valid Time	5	10*	
t_{H-DR}	Read Data Hold Time	4	8.5**	
t_{S-CSN}	Chip Select Setup Time	0	-	
t_{H-CSN}	Chip Select Hold Time	0	-	
t_{S-EF}	Empty Flag Set Time	-	10*	

OEN operations – Driving the bus permanently

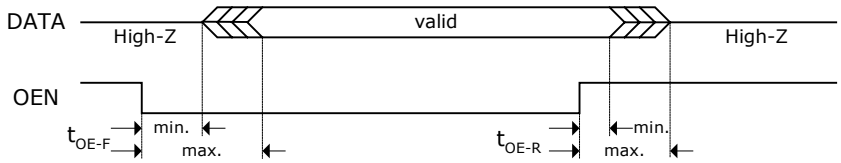


Figure 3

Spec	Description	Min (ns)	Max (ns)
t_{OE-F}	OEN Rise to Data Valid	1.5	9
t_{OE-R}	OEN Fall to Data Valid	1	8.5

Note: With OEN = Low the output buffers are driving allthe time, with OEN = High they are driving only during a read strobe. While writing to the TDC-GPX OEN has to be High.

Fake Reads for speeding up data readout

The maximum data readout rate is limited by the empty flag set time as it is not allowed to read from an empty FIFO. This can be overcome by a second fake read strobe which is delayed to the read strobe at the TDC-GPX.

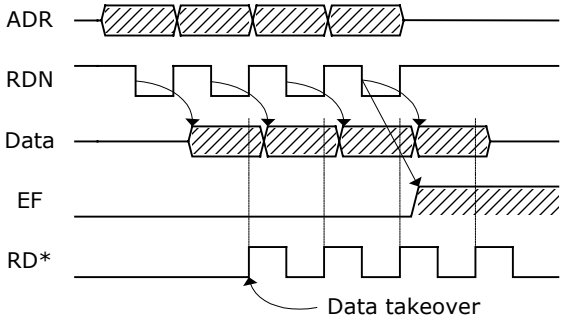


Figure 4

1.3.2 16 Bit Mode

The TDC-GPX data bus can be switched from 28 Bit to 16 Bit. This is done writing a 0x0000010 to address 14. After that all read / write commands have to be done in pairs. When reading the last data from an interface FIFO the empty flag disappears already with the first read command. Nonetheless it is mandatory to read a second time.

The first read/write command always refers to the LSW, the second one to the MSW. The highest 4 Bit of the MSW are not relevant (write) or shall be ignored (read).

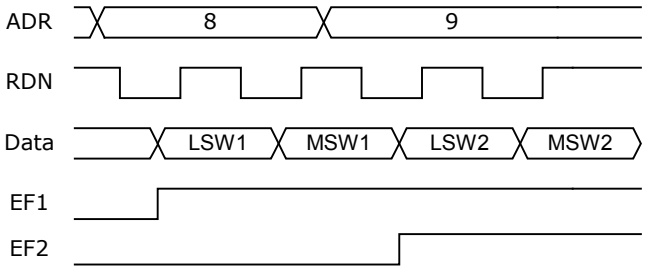


Figure 5

Note: See Bug-Report 01 at the end of the datasheet

1.3.3 Disable Timings

(Vddo = Vddc = 3.3 V, Ta = +25°C)

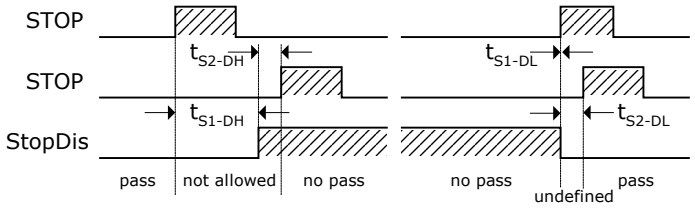


Figure 6

Spec	Description	Min (ns)	Max (ns)
t_{S1-DH}	Disable Setup Time	-	6
t_{S2-DH}	Disable Setup Time	-	1
t_{S1-DL}	Disable Hold Time	-	0
t_{S2-DL}	Disable Hold Time	-	2

1.3.4 Reset Timings

Power-up Reset: (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)	Max (ns)
t_{ph}	Reset pulse width	200	-

Master Reset: (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)	
t_{ph}	Reset pulse width	10	
t_{rfs}	Time after rising edge of reset pulse before hits are accepted	27	
t_{rrs}	Time after falling edge of reset pulse before hits are accepted	13	

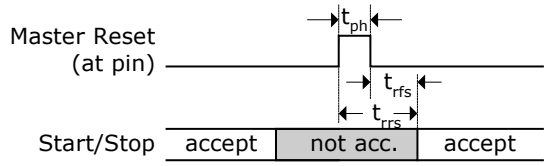


Figure 7

Partial Reset: (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)	
t_{ph}	Reset pulse width	10	
t_{rfs}	Time after rising edge of reset pulse before hits are accepted	60	
t_{rrs}	Time after falling edge of reset pulse before hits are accepted	13	
t_{rs}	Time berfore rising edge of reset pulse where hits will be lost	-	

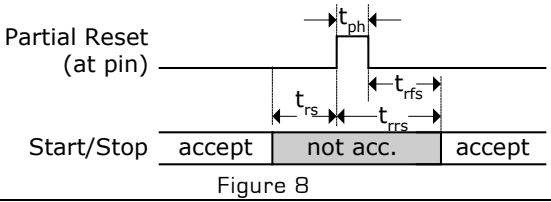


Figure 8

1.3.5 General Timings & Resolution

The TDC-GPX time measurement is based on internal propagation delays. Those delays depend on temperature and voltage. They also vary over the production lots. The resolution adjust mode (see) uses the voltage dependency to compensate for temperature and production variations and sets the circuits to a fixed and programmable resolution.

Figure 9 shows the dependency of all timings from the core voltage, referred to the 3.3V timings. The resolution at 3.3V can be varied by factors 0.93 at 3.6V to 1.4 at 2.3V.

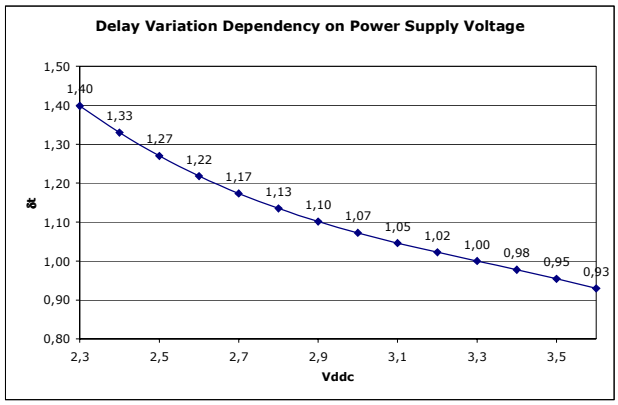


Figure 9

Figure 10 shows the dependency of all timings on the temperature, referred to 25°C junction temperature. If the temperature increases from 25°C to 70°C, the intrinsic resolution goes down by a factor 1.077. In resolution adjust mode this is compensated by increasing the core voltage from 3.3V to 3.6V.

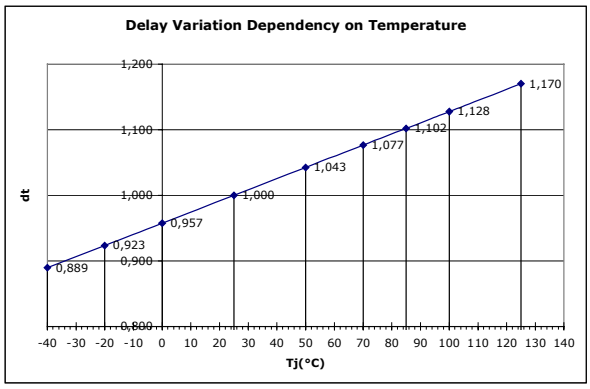


Figure 10

Without resolution adjust, the intrinsic resolution varies slightly from chip to chip. The distribution over the production lots is of gaussian type.

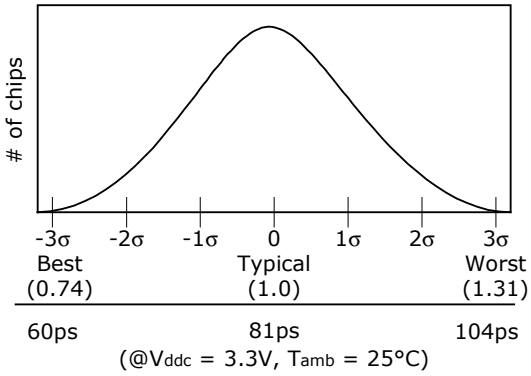


Figure 11

Within a single production lot the distribution is narrower. Figure 12 shows a typical distribution of the intrinsic resolution at 3.3 V core voltage and 25°C ambient temperature within a single production lot.

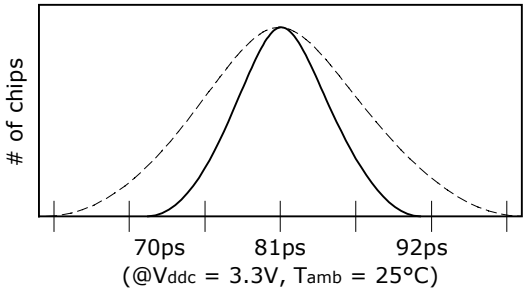


Figure 12

Example:

Taking the distribution from Figure 12 and assuming an operating temperature range of 0°C to 40°C as well as 1 Mhz data rate. The junction temperature will be about 57°C max. The slowest chips will have 92ps * 1.043 = 97ps resolution at 3.3V Vddc. Increasing the core voltage to 3.6V will speed them up to 90.2ps. Setting the resolution adjust mode to a resolution of 95ps will guarantee that the PLLs of all chips will lock at one and the same resolution over the whole operating temperature range.

1.4 Pin Description

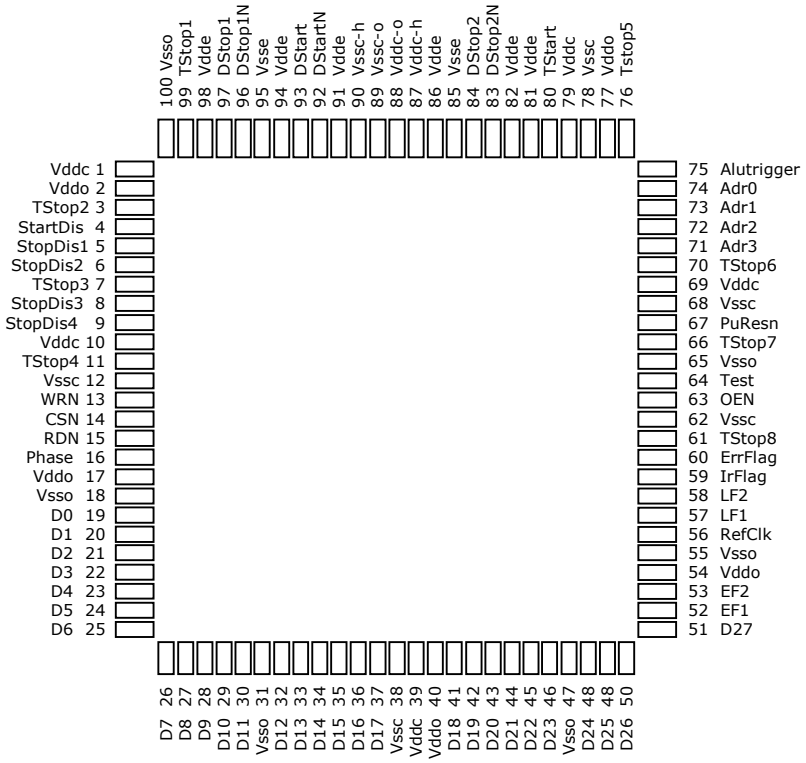


Figure 13

PIN No TQFP 100	PIN No TFBGA 120	PIN Name	Description	Type	Terminal () = if not used
001	A1	Vddc	Core supply voltage		Vddc
002	B1	Vddo	I/O supply voltage		Vddo
003	C1	Tstop2	TTL input 'Stop2'	TTL input	(10kΩ to GND)
004	C2	StartDis	Disable input 'DStart' or 'TStart'	TTL input	(GND)
005	D1	StopDis1	Disable input 'DStop1' or inputs 'TStop1 ' and 'TStop2'	TTL input	(GND)
006	C3	StopDis2	Disable input 'DStop2' or inputs 'TStop3 ' and 'TStop4'	TTL input	(GND)
007	D2	TStop3	TTL input Stop3	TTL input	(10kΩ to GND)
008	E1	StopDis3	Disable inputs 'TStop5 ' and 'TStop6'	TTL input	(GND)
009	D3	StopDis4	Disable or inputs 'TStop7 ' and 'TStop8'	TTL input	(GND)
010	F1	Vddc	Core supply voltage		Vddc
011	E3	TStop4	TTL input 'Stop4'	TTL input	(10kΩ to GND)
012	F2	Vssc	Core GND		GND
013	G1	WRN	Write (LOW active)	TTL input	
014	F3	CSN	Chip select (LOW active)	TTL input	(GND)
015	G2	RDN	Read (LOW active)	TTL input	
016	H1	Phase	Phase output PLL		

017	G3	Vddo	I/O supply voltage		Vddo
018	H2	Vsso	I/O GND		GND
019	J1	D0	Data 0	Bidirectional 4mA	10kΩ to GND
020	J2	D1	`	Bidirectional 4mA	10kΩ to GND
021	K1	D2	`	Bidirectional 4mA	10kΩ to GND
022	K2	D3	`	Bidirectional 4mA	10kΩ to GND
023	L1	D4	`	Bidirectional 4mA	10kΩ to GND
024	L2	D5	`	Bidirectional 4mA	10kΩ to GND
025	M1	D6	`	Bidirectional 4mA	10kΩ to GND
026	N2	D7	`	Bidirectional 4mA	10kΩ to GND
027	M2	D8	`	Bidirectional 4mA	10kΩ to GND
028	N3	D9	`	Bidirectional 4mA	10kΩ to GND
029	M3	D10	`	Bidirectional 4mA	10kΩ to GND
030	N4	D11	Data 11	Bidirectional 4mA	10kΩ to GND
031	M4	Vsso	I/O GND		GND
032	N5	D12	Data 12	Bidirectional 4mA	10kΩ to GND
033	L3	D13	`	Bidirectional 4mA	10kΩ to GND
034	M5	D14	`	Bidirectional 4mA	10kΩ to GND
035	N6	D15	`	Bidirectional 4mA	10kΩ to GND
036	M6	D16	`	Bidirectional 4mA	10kΩ to GND
037	N7	D17	Data 17	Bidirectional 4mA	10kΩ to GND
038	L5	Vssc	Core GND		GND
039	M7	Vddc	Core supply voltage		Vddc
040	L6	Vddo	I/O supply voltage		Vddo
041	M8	D18	Data 18	Bidirectional 4mA	10kΩ to GND
042	N9	D19	`	Bidirectional 4mA	10kΩ to GND
043	L7	D20	`	Bidirectional 4mA	10kΩ to GND
044	M9	D21	`	Bidirectional 4mA	10kΩ to GND
045	L8	D22	`	Bidirectional 4mA	10kΩ to GND
046	M10	D23	Data 23	Bidirectional 4mA	10kΩ to GND
047	L9	Vsso	I/O GND		
048	M11	D24	Data 24	Bidirectional 4mA	10kΩ to GND
049	N12	D25	`	Bidirectional 4mA	10kΩ to GND
050	L10	D26	`	Bidirectional 4mA	10kΩ to GND
051	M13	D27	Data 27	Bidirectional 4mA	10kΩ to GND
052	N13	EF1	Interface FIFO 1 empty flag, active HIGH	Output 4mA	
053	L13	EF2	Interface FIFO 2 empty flag, active HIGH	Output 4mA	
054	L12	Vddo	I/O supply voltage		Vddo
055	L11	Vsso	I/O GND		GND
056	K13	RefClk	Input reference clock	TTL input	
057	K12	LF1	Interface FIFO 1 load flag, active HIGH *	Output 1mA	
058	K11	LF2	Interface FIFO 2 load flag, active HIGH *	Output 1mA	
059	J13	IrFlag	Interrupt flag, active HIGH	Output 1mA	
060	J12	ErrFlag	Error flag, active HIGH	Output 1mA	
061	H13	Tstop8	TTL input ‚Stop8'	TTL input	(10kΩ to GND)
062	H12	Vssc	Core GND		GND
063	H11	OEN	Output enable, active LOW	TTL input	(10kΩ to GND)

* Valid only whileF13 it is not read

064	G11	Test	acam test input, connect it to GND !	TTL input	GND
065	F13	Vsso	I/O GND		GND
066	F12	Tstop7	TTL input ‚Stop7'	TTL input	(10kΩ to GND)
067	F11	PuResN	Power-up reset, low active	TTL input	
068	E13	Vssc	Core GND		GND
069	E12	Vddc	Core supply voltage		Vddc
070	D12	Tstop6	TTL input 'Stop6'	TTL input	(10kΩ to GND)
071	D13	Adr3	Address 3	TTL input	
072	E11	Adr2	Address 2	TTL input	
073	C13	Adr1	Address 1	TTL input	
074	C12	Adr0	Address 0	TTL input	
075	D11	AluTrigger	External ALU trigger	TTL input	(10kΩ to GND)
076	C11	Tstop5	TTL input 'Stop5'	TTL input	(10kΩ to GND)
077	A11	Vddo	I/O supply voltage		Vddo
078	C10	Vssc	Core GND		GND
079	B10	Vddc	Core supply voltage		Vddc
080	C9	Tstart	TTL input 'Start'	TTL input	(10kΩ to GND)
081	B9	Vdde	LVPECL supply voltage		Vdde
082	A9	Vdde	LVPECL supply voltage		Vdde
083	B8	DStop2N	Differential input 'Stop2' , neg	Differential input	(10kΩ to GND)
084	A8	DStop2	Differential input 'Stop2' , pos	Differential input	(10kΩ to GND)
085	C7	Vsse	LVPECL GND		GND
086	B7	Vdde	LVPECL supply voltage		Vdde
087	A7	Vddc-h	Hardmacro supply voltage		Vddc-h
088	C6	Vddc-o	Hardmacro supply voltage		Vddc-o
089	B6	Vssc-o	Hardmacro GND		GND
090	A6	Vssc-h	Hardmacro GND		GND
091	C5	Vdde	LVPECL supply voltage		Vdde
092	B5	DStartN	Differential input 'Start' , neg	Differential input	(10kΩ to GND)
093	A5	DStart	Differential input 'Start' , pos	Differential input	(10kΩ to GND)
094	C4	Vdde	LVPECL supply voltage		Vdde
095	B4	Vsse	LVPECL GND		GND
096	A4	Dstop1N	Differential input 'Stop1' , neg	Differential input	(10kΩ to GND)
097	B3	Dstop1	Differential input 'Stop1' , pos	Differential input	(10kΩ to GND)
098	A3	Vdde	LVPECL supply voltage		Vdde
099	B2	TStop1	TTL input 'Stop1'	TTL input	(10kΩ to GND)
100	A2	Vsso	I/O GND		GND

1.5 Package Drawings

TQFP100:

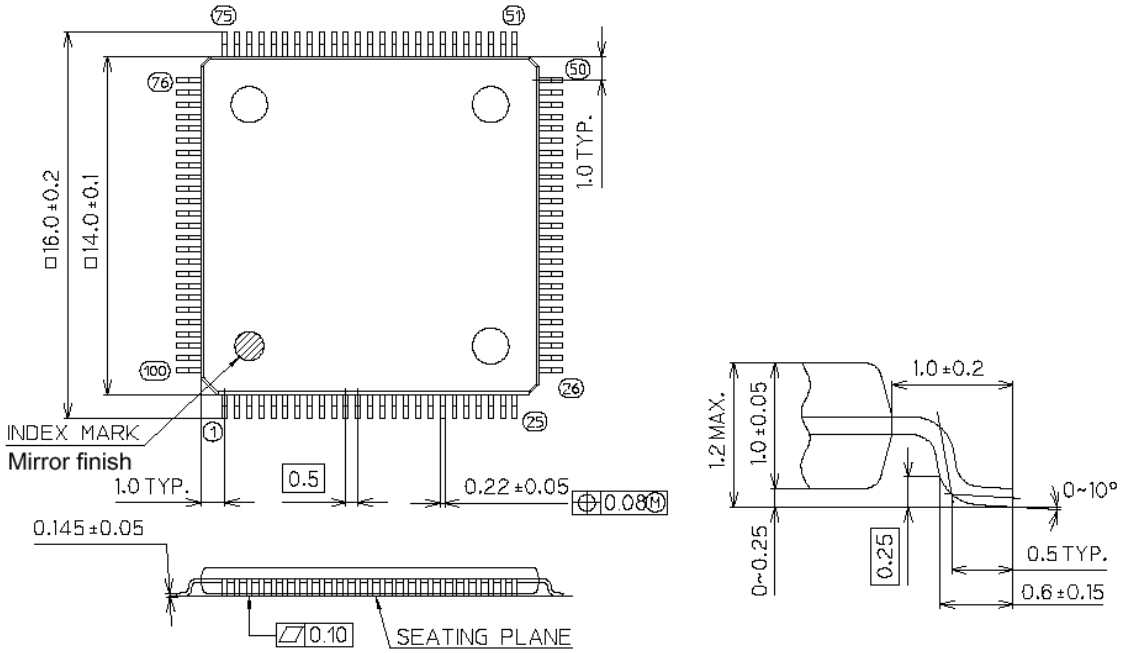
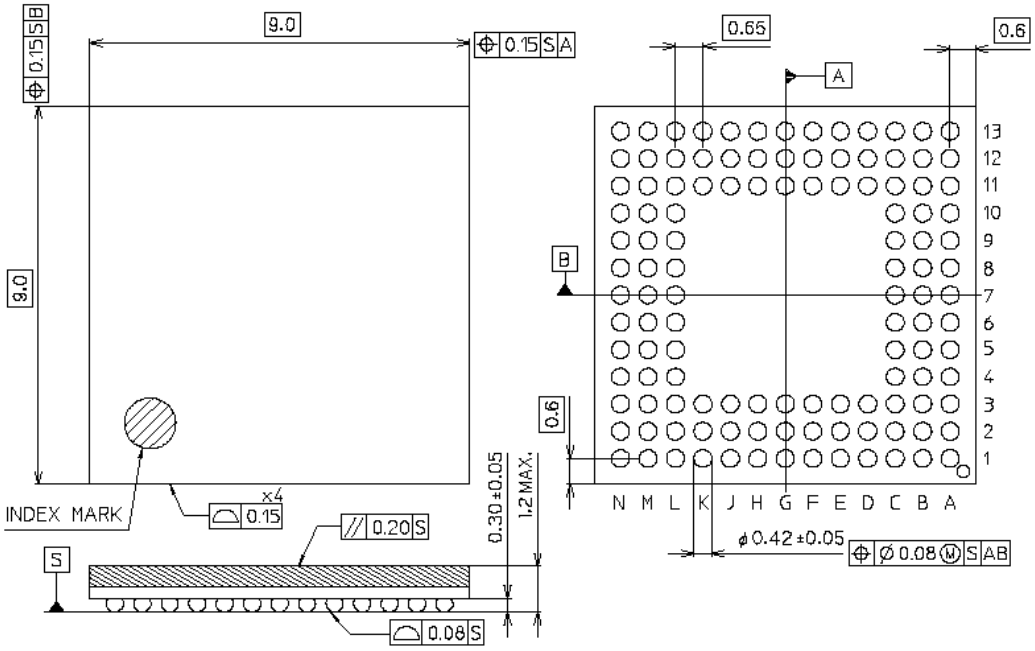


Figure 14

Sockets: E.g. Yamaichi IC149-100-025

TFBGA:



1.6 Power supply

1.6.1 Resolution adjust

In principle the high resolution of the TDC-GPX is derived from the internal gate propagation times. The gate propagation time depends upon voltage, temperature and the manufacturing process. Due to this dependency the resolution normally is not known and must be calculated via calibration measurements. In addition, the resolution is not stable, it sways with voltage and temperature. This does not apply using the resolution adjust mode for the TDC-GPX. In this mode the resolution of the TDC-GPX is adjusted quartz-accurately and absolutely temperature stable via Phase Locked Loop The phase locked loop (PLL) regulates the core voltage of the TDC-GPX so that the resolution is set exactly to the programmed value.

The BIN size is calculated as follows:

$$BIN_{I-Mode} = \frac{T_{ref} \times 2^{refclkdiv}}{216 \times hsdiv}$$

$$BIN_{G-Mode} = BIN_{I-Mode} \times \frac{1}{2}$$

$$BIN_{R-Mode} = BIN_{I-Mode} \times \frac{1}{3}$$

$$BIN_{M-Mode} = BIN_{R-Mode} \times \frac{1}{MSet + 1}$$

Tref = 25ns (40 MHz reference clock)
RefClkDiv, HSDiv → Register 7

The adjustment range of the resolution can reach values from –40 % up to +9 % of the normal resolution at 3.3 V and 25 °C. If environmental conditions lead to very large adjustments the locked-state can be lost. Then the PLL changes to floating resolution until the conditions allow the PLL to lock again.
Figure 15 shows the recommended external circuit for the regulation loop.

Note: See also application note AN013.

Example:
RefClkDiv = 7 and HSDiv = 183 give the following resolution:
I-Mode 80.9553 ps BIN
G-Mode 40.4776 ps BIN
R-Mode 26.9851 ps BIN

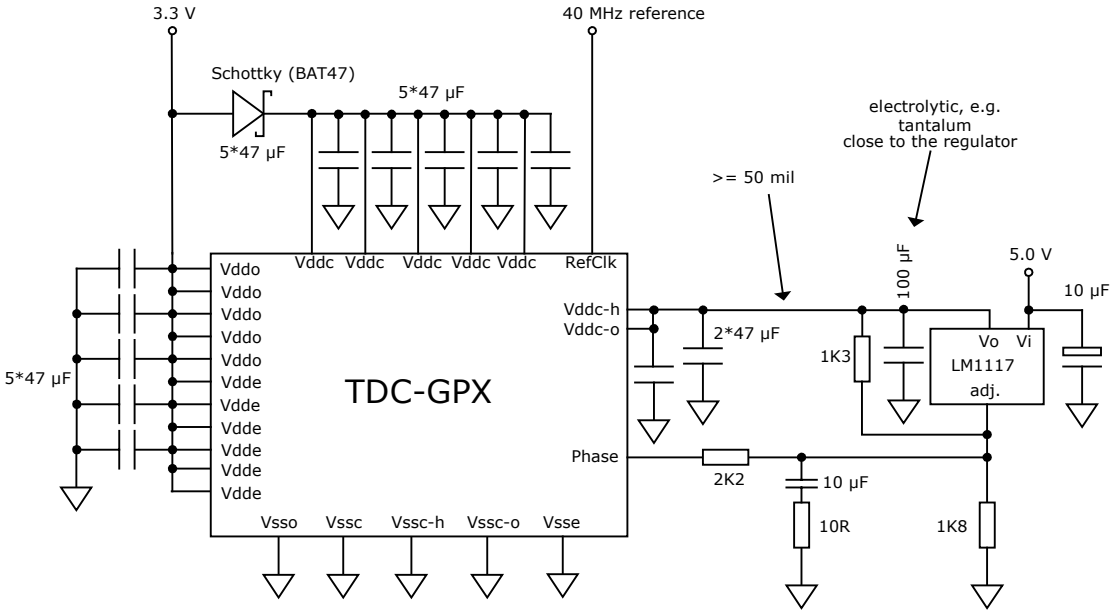


Figure 15

1.6.2 Supply voltages

Although the TDC-GPX is a fully digital circuit, some analog measures affect the circuit. The reason is that the TDC is based on the internal analog measure 'propagation delay time' which is influenced by temperature and supply voltage. A good layout of the supply voltage is essential for good measurement results. It should be high capacitive and of low inductance.

There are several connections for power supply provided at the TDC-GPX:

- Vddo - I/O supply voltage
- Vddc - Core supply voltage
- Vddc-h - Supply for the Hamac
- Vddc-o - Supply for the ring oscillator
- Vdde - Supply of LVPECL inputs
- Vsso - I/O GND
- Vssc - Core GND
- Vssc-h - Hamac GND
- Vssc-o - Ring oscillator GND

For a good stabilization we recommend the use of
5 * 47 µF, one for each Vddc pin.
1 * 47 µF for Vddc-h.
1 * 47 µF for Vddc-o.
5 * 47 µF, total for Vddo and Vdde.

Recommended capacitors:
Taiyo-Yuden LMK325BJ476MM, 47µF, 1210

The supply voltage for the core should not be higher than the supply voltage of the I/O plus 0.6 V. Otherwise the signal flow could be disturbed.
All ground pins should be connected to a ground plane on the printed circuit board.
Vddc, Vddc-h and Vddc-o are floating and are supplied from the resolution adjust voltage regulator.
Vddo should be provided by a fixed voltage regulator to avoid disturbances caused by the inputs supply.

Power consumption

The current consumption is about 45 mA in R- and G-mode and 39mA in I-mode idle plus 5 mA per million events. At 1 million continuous events per second the junction temperature will increase to 17 °C above ambient.
The thermal resistance Rth j-a is 96K/W (still air) for the TQFP package and 105K/W for the TFBGA package. With available heatsinks it can be reduced to 35k/W (still air), due to a very small Rthj-c of the package.
The maximum junction temperature is
Tj max = 125 °C.

1.6.3 Design Rules

As shown in Figure 15 the supply voltage of the measuring unit, Vddc-o/h, is provided by an adjustable linear regulator. It is strongly recommended to use only LM317 or LM1117 regulators, because only for these regulators the circuit is tested and approved. Do not use low drop regulators because these regulators' reference refers to the output voltage and the regulation might be in conflict with the PLL regulation. The input voltage of the regulator should be ≥ 5 V so that the maximum output voltage of the PLL regulation circuit is not limited by the voltage regulator's voltage drop of 1.2 V to 1.3 V.

Also for the other supply voltages, Vddc, Vddo & Vdde, linear regulators are recommended. Switched mode regulators will introduce a lot of noise to the measurement.

The width of the strip line between the regulator's output and the TDC-GPX power supply pins should be at least 50 mil.

For more detailed information concerning the PLL regulation circuit please refer to application note no. 13 at the end of this document.

1.7 Register settings

In depends on the operating mode whether bits are relevant or not. Especially the read data structure depends on the operating mode.

1.7.1 Write Registers

Service bits are for acam testing and security purposes only, Please use the recommended values.
These registers can also be read back.

Register 0: Adr = 0			I	G	R	M
0	ROsc	'1' = start ring oscillator	x	x	x	x
1	RiseEn0	'1' enable rising edge sensitivity on DStart input		x	x	x
2	FallEn0	'1' enable falling edge sensitivity on DStart input		x	x	x
3	RiseEn1	'1' enable rising edge sensitivity on DStop1 input		x	x	x
4	FallEn1	'1' enable falling edge sensitivity on DStop1 input		x	x	x
5	RiseEn2	'1' enable rising edge sensitivity on DStop2 input		x	x	x
6	FallEn2	'1' enable falling edge sensitivity on DStop2 input		x	x	x
7 – 9	HQSel	Service bits, must be set to '001'	x	x	x	x
10 – 18	TRiseEn	'1' enables rising edges for the TTL inputs Bit 10 = TStart, Bit 11 = TStop1 … Bit 18 = TStop8	x			
19 – 27	TFallEn	'1' enables falling edges for the TTL inputs Bit 19 = TStart, Bit 20 = TStop1 … Bit 27 = TStop8	x			

Register 1: Adr = 1			I	G	R	M
0 – 3	Adj0	Channel adjustment bits channel 0 (Start)		x	x	x
4 – 7	Adj1	Channel adjustment bits channel 1 (R-Mode = 2, G-Mode = 0)		x	x	x
8 – 11	Adj2	Channel adjustment bits channel 2 (R-Mode = 6, G-Mode = 5)		x	x	x
12 – 15	Adj3	Channel adjustment bits channel 3 (R-Mode = 0, G-Mode = 0)		x	x	x
16 – 19	Adj4	Channel adjustment bits channel 4 (R-Mode = 2, G-Mode = 5)		x	x	x
20 – 23	Adj5	Channel adjustment bits channel 5 (R-Mode = 6, G-Mode = 0)		x	x	x
24 – 27	Adj6	Channel adjustment bits channel 6 (R-Mode = 0, G-Mode = 5)		x	x	x

Adjustment bits recommendation:
R-Mode: Adj1 = Adj4 = Adj7 = 2, Adj 2 = Adj 8 = 6, Adj5 = 6
G-Mode: Adj2 = Adj4 = Adj6 = Adj8 = 5.

Register 2: Adr = 2			I	G	R	M
0	G-Mode	'1' = switch on G-Mode		x		
1	I-Mode	'1' = switch on I-Mode	x			
2	R-Mode	'1' = switch on R-Mode			x	x
3 – 11	Disable	'1' = disable channel Bit 3 = channel 0 (Start) … Bit 11 = channel 8	x	x	x	x
12 – 15	Adj7	Channel adjustment bits channel 7 (R-Mode = 2, G-Mode = 0)		x	x	x
16 – 19	Adj8	Channel adjustment bits channel 8 (R-Mode = 6, G-Mode = 5)		x	x	x
20 – 21	DelRise1	Service bits, set '0'		x	x	
22 – 23	DelFall1	Service bits, set '0'		x	x	
24 – 25	DelRise2	Service bits, set '0'		x	x	
26 – 27	DelFall2	Service bits, set '0'		x	x	

Register 3: Adr = 3			I	G	R	M
0 – 4	MSet	Setting resolution factors 1 to 31 in M-Mode				x
5 – 6	DelT1	Service bits, set '0'		x	x	
7 – 8	DelT2	Service bits, set '0'		x	x	
9 – 10	DelT3	Service bits, set '0'		x	x	
11 – 12	DelT4	Service bits, set '0'		x	x	
13 – 14	DelT5	Service bits, set '0'		x	x	
15 – 16	DelT6	Service bits, set '0'		x	x	
17 – 18	DelT7	Service bits, set '0'		x	x	
19 – 20	DelT8	Service bits, set '0'		x	x	
21 – 22	RaSpeed0	Service bits, set '0'		x	x	
23 – 24	RaSpeed1	Service bits, set '0'		x	x	
25 – 26	RaSpeed2	Service bits, set '0'		x	x	
27	GTest	Switches TStart to DStart, TStop1 to DStop1 and TStop2 to DStop2 (TTL to ECL, testing in G-Mode)		x	x	x

Register 4: Adr = 4			I	G	R	M
0 – 7	StartTimer	defines repetition rate of internal Start in (N + 1)*Tref recommended: 5 µs ((199 + 1) * 25ns)	x			
8	Quiet	'1' = Switch on Quiet Mode in G-, R- or M-Mode If Quiet is set to '1', the ALU doesn't start automatically, but after a rising edge at pin ALUTrigger or after writing '1' into Bit 'AluTrigSoft' (mandatory in M-Mode)		x	x	x
9	Mon	Switch on M-Mode				x
10 – 11	RaSpeed3	Pulse-pair timing adjust, typically set '0'		x	x	x
12 – 13	RaSpeed4	Pulse-pair timing adjust, typically set '0'		x	x	x
14 – 15	RaSpeed5	Pulse-pair timing adjust, typically set '0'		x	x	x
16 – 17	RaSpeed6	Pulse-pair timing adjust, typically set '0'		x	x	x
18 – 19	RaSpeed7	Pulse-pair timing adjust, typically set '0'		x	x	x
20 – 21	RaSpeed8	Pulse-pair timing adjust, typically set '0'		x	x	x
22	MasterReset	'1' = general reset excluding configuration registers	x	x	x	x
23	PartialReset	'1' = general reset excluding configuration registers and Interface FIFO content	x	x	x	x
24	AluTrigSoft	Starts ALU in Quiet Mode		x	x	x
25	EFlagHiZN	'1' = EF output pin is driving all the time	x	x	x	x
26	MTimerStart	'1' = the internal MTimer is started with a Start pulse	x	x	x	x
27	MTimerStop	'1' = the internal MTimer is started with a Stop pulse	x	x	x	x

Register 5: Adr = 5			I	G	R	M
0 – 17	StartOff1	programmable internal Start-offset	x	x	x	x
18 – 20	ServiceMAdj	Service bits, set "0"				x
21	StopDisStart	Stop disable before a Start pulse	x	x	x	x
22	StartDisStart	Start disable after a Start pulse		x	x	x
23	MasterAluTrig	Master reset by Alutrigger pin HIGH (only with no Quiet Mode)	x	x	x	
24	PartialAluTrig	Partial reset by Alutrigger pin HIGH (only with no Quiet Mode)	x	x	x	
25	MasterOenTrig	Master reset by OEN pin LOW (only with OEN not used)	x	x	x	x
26	PartialOenTrig	Partial reset by OEN pin LOW (only with OEN not used)	x	x	x	x
27	StartRetrig	Start retrigger	x	x	x	

Register 6: Adr = 6			I	G	R	M
0 – 7	Fill	Defines the level when the fill-level Flags LFx of the 2 interface FIFOs will be set.	x	x	x	
8 – 25	StartOff2	programmable internal Start-offset (in G-Mode only)		x		
26	InSelECL	select ECL inputs for I-Mode DStop1 -> TStop1, TStop3, TStop5, TStop7 DSTop2 -> TStop2, TStop4, TStop6, TStop8(single channels can be switched off using 'Disable'	x			
27	PowerOnECL	'1' = Switch-on power for ECL-inputs	x	x	x	x

When reading back register 6 the "Fill" bits 0 to 7 will be inverted.

Register 7: Adr = 7			I	G	R	M
0 – 7	HSDiv	High speed divider PLL	x	x	x	x
8 – 10	RefClkDiv	Reference clock divider PLL	x	x	x	x
11	ResAdj	Switch-on resolution adjust mode	x	x	x	x
12	NegPhase	Invert phase output of PLL	x	x	x	x
13	Track	cut regulation loop of PLL	x	x	x	x
14	Service	Service Bits, set '0'				
15 – 27	MTimer	Setting internal timer in multiples of Tref, 0 – 8191	x	x	x	x

Register 14: Adr = 14			I	G	R	
0 – 3	Service	Write "0"	x	x	x	x
4	16BitMode	'1' switches on the 16 Bit mode of the data bus	x	x	x	x
5 – 27	Service	Write "0"	x	x	x	x

After 16 Bit mode is set all further read/write commands have to be done in pairs of 16 Bit.

1.7.2 Read registers

- **I-Mode**

Register 8: Adr = 8		
0 – 16	IFIFO1	Time interval data from Interface FIFO1, Hit = Stop-Start
17	Slope1	Slope of this hit
18 – 25	Start#1	Start number of this hit
26 – 27	ChaCode1	Channel code of this hit

Register 9: Adr = 9		
0 – 16	IFIFO2	Time interval data from Interface FIFO2, Hit = Stop-Start
17	Slope2	Slope of this hit
18 – 25	Start#2	Start number of this hit
26 – 27	ChaCode2	Channel code of this hit

Register 10: Adr = 10		
0 – 16	StartO1	Time interval between external start and first internal start
17 – 27	-	not used

- **G-Mode**

Register 8: Adr = 8		
0 – 21	IFIFO1	Time interval data from Interface FIFO1, Hit = Stop-Start
22	Slope1	0 = falling edge, 1 = rising edge
23 – 27	-	not used

Register 9: Adr = 9		
0 – 21	IFIFO2	Time interval data from Interface FIFO2, Hit = Stop-Start
22	Slope2	0 = falling edge, 1 = rising edge
23 – 27	-	not used

Register 10: Adr = 10		
0 – 15	-	not used
16 – 27	-	not used

- **R-Mode & M-Mode**

Register 8: Adr = 8		
0 – 22	IFIFO1	Time interval data from Interface FIFO1, Hit = Stop-Start
23 – 27	-	not used

Register 9: Adr = 9		
0 – 22	IFIFO2	Time interval data from Interface FIFO2, Hit = Stop-Start
23 – 27	-	not used

Register 10: Adr = 10		
0 – 15	-	not used
16 – 27	-	not used

1.7.3 Read/Write registers

Register 11: Adr = 11			
0 – 7	StopCounter0	# of hits on DStop1, I-Mode: not available G-Mode: counting falling edge R-Mode: counting rising edge	read only
8 – 15	StopCounter1	# of hits on DStop2, I-Mode: not available G-Mode: counting falling edge R-Mode: counting rising edge	read only
16 – 23	HFifoErrU	'1' unmasks full flags of Hit FIFOs to ErrFlag pin	read/write
24 – 25	IFifoErrU	'1' unmasks full flags of Interface FIFOs to ErrFlag pin	read/write
26	NotLockErrU	'1' unmasks 'PLL not locked' to ErrFlag pin	read/write

Register 12: Adr = 12			
0 – 7	HFifoFull	Full flags of Hit FIFOs	read only
8 – 9	IFifoFull	Full flags of Interface FIFOs	read only
10	NotLocked	'PLL not locked' flag	read only
11	HFifoE	Falg indicating that all Hit FIFOs are empty	read only
12	TimerFlag	Flag indicating end of MTimer	read only
13 – 20	HFifoIntU	'1' unmasks full flags of Hit FIFOs to IntFlag pin	read/write
21 – 22	IFifoIntU	'1' unmasks full flags of Interface FIFOs to IntFlag pin	read/write
23	NotLockIntU	'1' unmasks 'PLL not locked' to IntFlag pin	read/write
24	HFifioEU	'1' unmasks 'All Hit FIFOs empty' to IntFlag pin	read/write
25	TimerFlagU	'1' unmasks end of MTimer to IntFlag pin	read/write
26	Start#U	'1' unmasks highest bit of Start# (I-Mode) to IntFlag pin	read/write
27	Service	Set to "0"	read/write

HFifoFull and IFifoFull will be set back to "0" when reading register 12. They are re-activated by a master reset or a partial reset.

2 I-Mode

2.1 Block diagram I-Mode

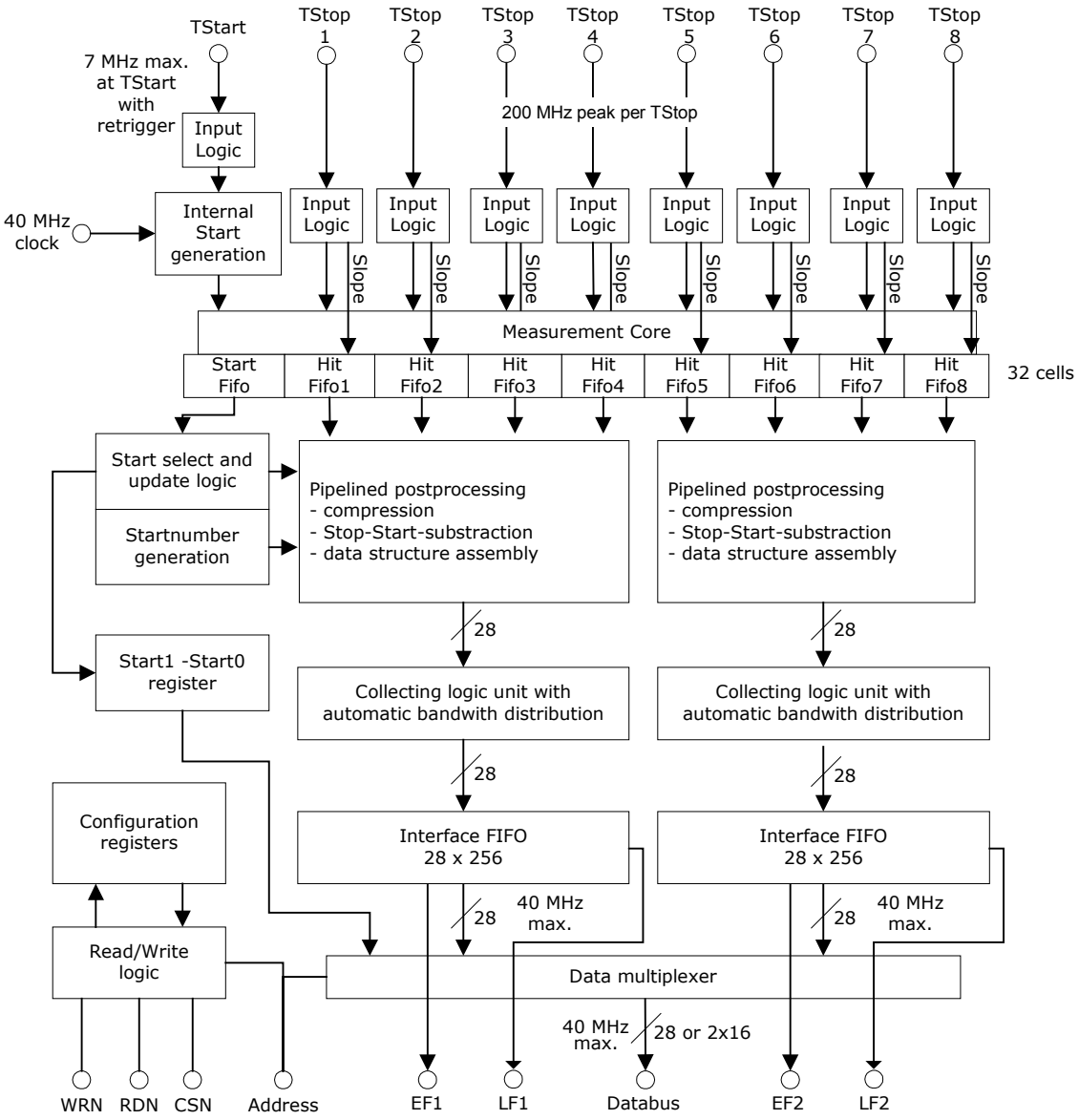


Figure 16: Block diagram

2.2 Input circuitry I-Mode

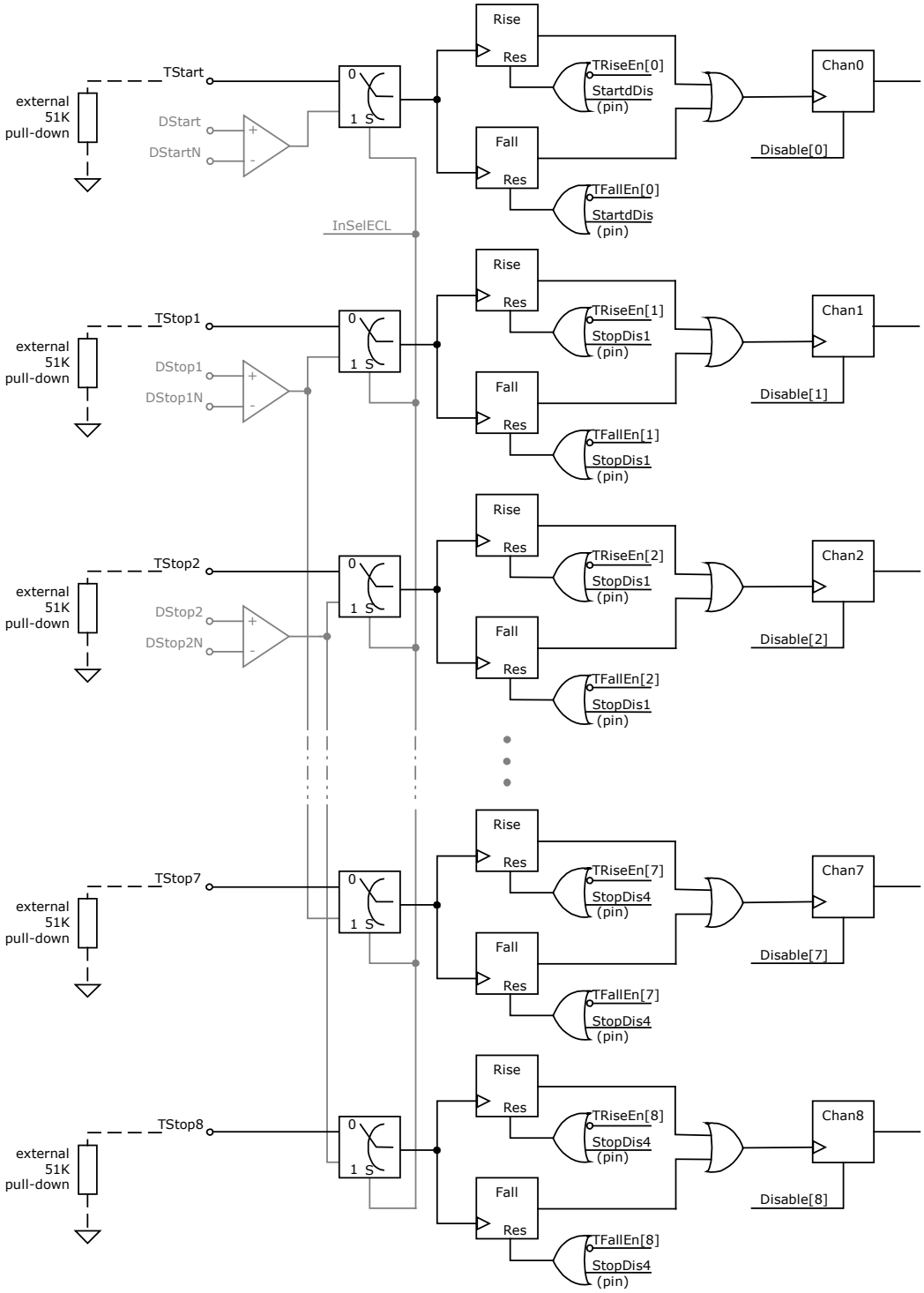


Figure 17: Input circuitry

2.3 I-Mode Basics

In this mode TDC-GPX offers

- 8 stop channels referring to 1 start channel,
- Each of typ. 81 ps resolution
- 5.5 ns pulse-pair resolution
- Start-retrigger up to 7 MHz
- Unlimited measuring range with internal start retrigger
- All inputs of LVTTL type
- Selectable rising/falling edge sensitivity for all channels
- Several disable possibilities for all channels

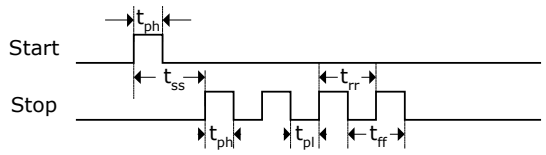


Figure 18: Measurement timings

Par.	Time (Condition) Min.	Max.	Description
t_{ph}	1.5 ns		Positive pulse width
t_{pl}	1.5 ns		Negative pulse width
t_{ss}	0 ns min **5.2 ns	9.4 µs *unlimited	Start to Stop
t_{rr}	5.5 ns (typ.)		Rising edge to rising edge
t_{ff}	5.5 ns (typ.)		Falling edge to falling edge

*with int. start retrigger **with StopDisStart = 1

Input circuitry

The detailed input structure is shown in Figure 17: Input circuitry. Each input separately can be set to be sensitive to rising or falling edge. This is done in register0, TRiseEn[8...0] and TFallEn[8...0]. The LSB stands for the TStart input, the MSB TStop8 input. A zero in the channel bit for TRiseEn and TfallEn at the same time disables the channel.

All inputs can be disabled by hardware, the stop inputs in pairs (pin 'StopDis1' disables inputs TStop1 and TStop2, etc.). They also can be disabled by Software setting the 'Disable' bits in register 2. The TDC-GPX offers the possibility to disable the Stop inputs automatically until a Start is coming in. This is set by StopDisStart = '1' in register 5.

Start Retrigger

After an initial start event, the TDC-GPX can generate its own internal starts. This is controlled by the parameter "StartTimer" in register 4. The start retrigger rate may not exceed 7 MHz.

Single Start

StartTimer = 0 switches off the internal Start generation. In this mode the measuring range is limited to 2^{17} BIN ≈ 10.6 µs (@ BIN = 81 ps). Further pulses at TStart will be ignored.

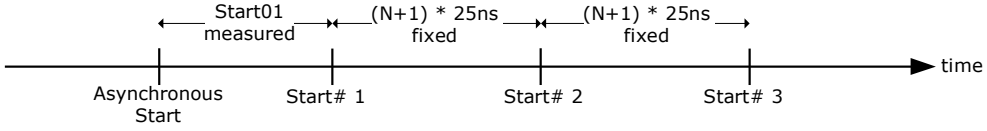
Internal Start Retrigger

The period of the start repetition is programmable in multiples of the 40 MHz reference clock between (4+1) and (255+1) x 25ns (Register 4: StartTimer[7...0]).
The time interval between the initial, external start and the first internal one will vary. It is therefore measured and stored as 'Start01' in register 10. It can be read out from this register as a 17 Bit integer in multiples of BIN.
The time intervals between following starts are fixed and referred to as (N +1) x Tref. Additionally, there is an 8 Bit counter for the start number (Start#). The start number is added to the output data.
A further option is to feed the highest bit of the Start counter to the IrFlag output pin by setting register 11, Bit 26 Start#U to one. With this signal the intenal start number counter can externally be extended to any size.
The internal start retrigger allows an **unlimited measuring range** for the TDC-GPX.

External Start Retrigger

A further option is to retrigger the Start externally. This option is activated by setting StartTimer = 1 (Reg 4) and StartRetrig = 1 (Reg 5). The further behavior is the same as for the internal start retrigger. The maximum retrigger frequency is typically 7 MHz. The time interval between two Starts is measured and stored in the "Start01" register. This value is reasonable only if the delay between two Start pulses does not exceed the measuring range of 2^{17} BIN ≈ 10.6 µs.

Figure 19



Start-Offset
For several reasons a mathematical offset is added to the stop time. One reason is to allow handling Start-Stop intervals down to 0 and even less. This 'StartOff1' is set in register 5 in multiples of BIN and it is 18 Bit wide. Internally the start offset is added to the time measurement result and has to be subtracted from the value read from the TDC. The other reason is to allo the ALU to look "into the past" without handling negative values (which the ALU could not do).

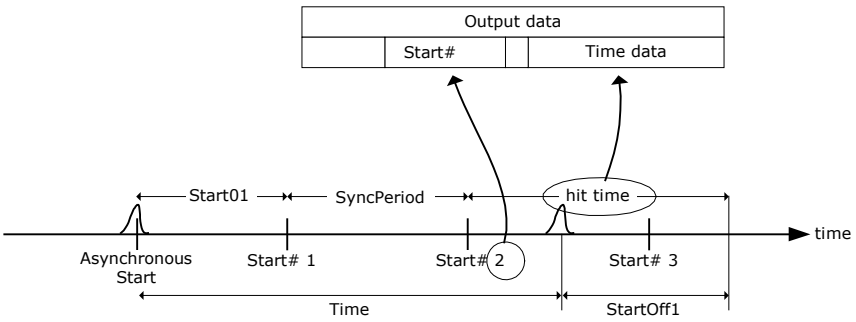


Figure 20

The real time interval Start to Stop is calculated from the output data as (Start# >0):

Time = (hittime - StartOff1 + Start01) * resolution +
(Start# - 1) * (StartTimer +1) * Tref

Adjusting the Start-Offset
The Start-Offset register of the TDC-GPX allows the compensation for the offset due to the different internal delays. It allows to do measurements down to 0 ns time intervals between Start and Stop. The correct setting should be done by experiment.

Procedure for single start applications:

1. Set StartOff1 = 0
2. Apply Start and Stop signals with a short delay (e.g. 12ns)
3. Step down the interval and look at the output data. They are getting smaller and smaller until you pass the internal Start time stamp. The output data then jumps to a very high value.
4. Take the time interval t_{cross} (from your generator) where this happens
5. Calculate StartOff1 = t_{cross} / BIN and write this value into register 5, StartOff1. In case you expect negative values add an additional amount X to StartOff1 and substract this value later on from your output data

With start retrigger the value StartOff1 should be set to

StartOff1 = 2,000 (≈ 162 ns).

The reason is that the ALU is internally stopped for about 50 ns during a start retrigger to add the new start time stamp. If there is a hit on each channel during this period the ALU will need
4 x 25 ns + 50 ns = 150 ns to transfer those data to the IFIFO. The ALU cannot handle negative values. Therefore the start offset is added so that the ALU can handle the data being collected during the break. In case the input data rate is higher (bursts) it will be necessary to increase also the offset value , e.g. to 10,000.

The start retrigger adds some indeterminacy – due to the 25ns reference – to whether a stop refers to the old start or the new one. This is not an uncertainty. Each time stamp that is negative after offset substraction can be remapped to the old start by adding the start period and reducing the start number by 1.

StopDisStart & StartDisStop
By default the Start and Stop inputs of the TDC-GPX are open immediately after a reset.

The consequence for the Stop channels is that even hits coming before a Start pulse will be measured. The bit StopDisStart in register 5 disables the Stop channels until there is a Start pulse. A consequence is that there is a minimum delay of 7 ns after the Start before hits are accepted on the Stop channels.

With single-start and internal start-retrigger only the first Start pulse is used for the measurement. In cases where more than one Start pulse is expected this might cause an overflow of the Hit FIFO of the Start channel. This will produce garbage data. There we recommend setting the StartDisStart bit in register 5. A '1' disables the Start channel after the first Start pulse.

Internal Data Processing
The raw values of the stop events are stored in 32-stage Hit FIFOs. One bit is added indicating the slope of the signal. This Hit FIFO can be filled with data at a peak rate of 182 MHz.

The following pipelined post-processing unit is responsible for compression, Start selection, correct Stop-Start subtraction and adding the start number to the output data. Subsequently a collection unit transfers

the data to the Interface FIFO, which is 256 stages deep. This is done with respect to automatic bandwidth distribution. If a hit from one channel has been processed, the neighbored channel gets highest priority for next operation. If there is no hit on the next, the next sequential gets priority and so on. The maximum rate for transfer into the Interface FIFO is 40 MHz. So if there are hits on all channels equally distributed, the maximum rate per channel is 10 MHz. If there are hits on only one channel, this channel has 40 MHz maximum rate.

Finally a data multiplexer adds data from both Interface FIFOs to the data bus. The data bus is 28 Bits wide and capable of 40 MHz transfer rate. The data bus can be switched to 16 Bit width writing 0x0000010 into address 14. A LOW at pin 'Output enable' forces the bidirectional bus drivers to permanent output state. This is helpful for fast data read out routines.
Each Interface FIFO has an empty flag (EF) and a load-level flag (LF). All flags are HIGH active. At low data rates it is recommended to check the EF to see whether there are data available for read out. It is not allowed to read from an empty Interface FIFO. The LF is helpful at high data rates. The load level threshold can be set in 'Fill' in register 6 and is the same for both FIFOs. As soon as the set number of data is available this can be read from the FIFO as a block without the need of checking the EF.
Note: the load-level flags are not synchronized. The load-level flag for a FIFO is valid only if it is **not** read from this FIFO. Otherwise there might be spikes.

2.4 Data structure

The output data are integers with a BIN width defined by the setting of the resolution adjust unit (1.6.1 Resolution adjust),

$$BIN = \frac{T_{ref} \times 2^{refclkdiv}}{216 \times hsdiv}$$

Bits 27...26	Bits 25...18	Bit 17	Bits 16...0
Channel code	Start# = Start number	Slope	Time interval data Hit = Stop-Start

The time interval is calculated (externally) as:
If Start# is 0:
Time = 1 BIN(ps) * (Hit – StartOff1)
If Start# > 0:
Time = 1 BIN(ps) * (Hit – StartOff1 + StartO1 + (Start# - 1) * (StartTimer +1) * Tref

2.5 Reset

There are 3 ways of resetting the device:

- **Power-up reset**: a low signal at pin PURESN resets the whole chip.
- **Master-Reset**: this command resets everything except the configuration registers. It can be done by software writing to register 4. When MasterAluTrig in register 5 is set to '1' it can be done also by a HIGH at the Alutrigger input pin.
- **Partial-Reset**: this command resets everything except the configuration registers and the Interface FIFOs. It can be done by software writing to register 4. When PartialAluTrig in register 5 is set to '1' it can be done also by a HIGH at the Alutrigger input pin.

After a Power-on reset and a Master reset it takes 40 ns before the Start and Stop inputs accept data.
After a Partial reset it takes 75 ns before the Start and Stop inputs accept data.

2.6 MTimer

There is an internal timer available for internal use. The main application will be setting a dedicated time interval between 25ns and 204.7 µs after which the interrupt flag is set. The period is set in 'MTimer', register 7, in multiples of Tref. The maximum delay is 8191 * Tref = 204.7 µs. The timer can be started by a Stop and/or Start signal. This is set in 'MTimerStart' and 'MTimerStop', register 4. Setting Bit 'TimerFlag', register 12, the interrupt flag is set when the timer stops.

2.7 Interrupt Flag

The user can select on which event(s) the interrupt flag is set.
The selection is done in register 12, Bits 13 to 25, by unmasking the dedicated bits. They are combined by an Or-Gate to the interrupt flag.
Selectable events are

- Hit FIFOs 1, 2 ...or/and 8 are full
- Interface FIFOs 1 or/and 2 are full
- PLL not locked
- All Hit FIFOs empty
- End of Mtimer

2.8 Error Flag

The user can select on which event(s) the error flag is set.
The selection is done in register 11, Bits 16 to 26, by unmasking the dedicated bits. They are combined by an Or-Gate to the error flag.
Selectable events are

- Hit FIFOs 1, 2 ...or/and 8 are full
- Interface FIFOs 1, 2 ...or/and 8 are full
- PLL not locked

2.9 Differential Inputs

It is possible to use the differential inputs also in I-Mode. Setting register 6, InSelECL= '1' switches the measurement channels to the two available differential inputs.
The power for the differential inputs has to be switched on separately by setting register 6, Power-OnECL = '1'.

2.10 I-Mode Timing & Resolution

The delay parameters vary with voltage, temperature and process tolerance. The following table lists the derating factors.

Derating by	Minimal	Maximal
Voltage	0.91 at 3.6V	1.2 at 2.85V
Temperature	0.889 at –40°C	1.17 at +125°C
Process	0.74 at BC	1.31 at WC

With the stabilization of the resolution by the resolution adjust mode, the voltage of the core decreases with decreasing temperature, and increases with increasing temperature. The setting should be done in a way that at maximum operating temperature the maximum core voltage is reached, and that minimum core voltage is reached at minimum operating temperature. With this method you get two limits:

Best case process, deepest temperature, lowest voltage: 0.74 x 0.889 x 1.2 = 0.789
Worst case process, highest temperature, highest voltage: 1.31 x 1.17 x 0.91 = 1.394

With a typical resolution of 81 ps (typ. process, 25°C, 3.3 V) you get two limits for the resolution:

	Best	Worst
Resolution	64 ps	113 ps

The BIN or LSB width is defined by the setting of the resolution adjust unit (1.6.1 Resolution adjust),

The standard deviation (1 σ) of the result is typically 0.9 LSB + 2,5ps * Δt/µs.

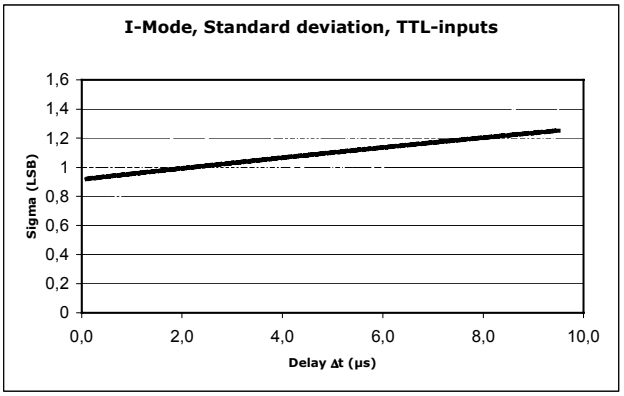


Figure 21

DNL
the TDC-GPX shows a moderate differential non-linearity (DNL) because internal propagation delays were used for the time measurement and because those delays are different for rising and falling edges. But the variation from channel to channel is strongly systematic. The following diagram shows the DNL data at a resolution of 74 ps:

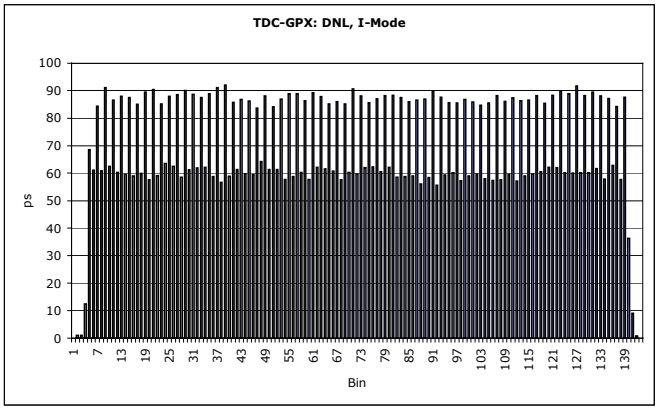


Figure 22: DNL

INL
The integral non-linearity describes the deviation over the full measuring range. The INL of the TDC-GPX for a single Start-Stop measurement with a delay > 6 ns is below our measurement capability and can be neglected. In the close-up region below 6 ns the deviation is about 100 ps.

2.11 Measurement Flow

In the following we show two typical examples of register settings and measurement flow in I-Mode.

2.11.1 Single measurement

Task:
Measuring 8 channels within a window of 2 µs from Start.

```
//****** I-Mode, Stops against single Start **********

PuResN=Low;                         // Power-up reset
PuResN=High;

StopDis1 = High;                    // Disable inputs
StopDis2 = High;
StopDis3 = High;
StopDis4 = High;
                                    // write configuration registers:
_oupd( 0,0x007FC81);                // Rising edges, Start ringoscil.
_oupd( 1,0x0000000);
_oupd( 2,0x0000002);                // I-Mode
_oupd( 3,0x0000000);
_oupd( 4,0x6000000);                // Mtimes trig. by Start, EFlagHiZN
_oupd( 5,0x0E004DA);       //StopDisStart, StartDisStart, StartOff1 = 100ns, MasterAluTrig
_oupd( 6,0x0000000);
_oupd( 7,0x0281FB4);                // Res = 82.3045ps
_oupd(11,0x7FF0000);                // Any error -> ErrFlag
_oupd(12,0x2000000);                // Mtimer -> IrFlag
_oupd(14,0x0000000);

_oupd( 4,0x6400000);                // Master reset

StopDis1 = Low;                     // Enable inputs
StopDis2 = Low;
StopDis3 = Low;
StopDis4 = Low;

do
{
   while(IrFlag=Low);                           // Check interrupt flag

   while((EF1=Low)or(EF2=Low))                  // Check empty flag
   {
      if (EF1=Low)                              // Data on IFIFO1?
      {
         data = _inpd(8);                       // Read IFIFO1
         Chan = (data & 0xC000000)>>26 + 1;           // Get channel#
         Time = (data & 0x1FFFF);               // Get time Stop-Start
         Printf(Chan,time);
      }
      if (EF2=Low)                              // Data on IFIFO2?
      {
         data = _inpd(9);                       // Read IFIFO2
         Chan = ((data & 0xC000000)>>26) + 5;   // Get channel#
         Time = (data & 0x1FFFF);               // Get time Stop-Start
         Printf(Chan,time);
      }
   }

   Alutrigger = High;                           // Master reset
   Alutrigger = Low;

} while(!quit)
```

2.11.2 Continous Measurement

Task: Typical application fluorescence spectroscopy.
Measuring a continous signal stream using the internal start-retrigger.

```
//****** I-Mode, endless measurement range with internal start retrigger **********
PuResN=Low;                         // Power-up reset
PuResN=High;
StopDis1 = High;                    // Disable inputs
StopDis2 = High;
StopDis3 = High;
StopDis4 = High;
                                    // write configuration registers:
_oupd( 0,0x007FC81);                // Rising edges, Start ringoscil.
_oupd( 1,0x0000000);
_oupd( 2,0x0000002);                // I-Mode
_oupd( 3,0x0000000);
_oupd( 4,0x2000027);                // StartTimer = 39 -> period = 1µs, EFlagHiZN
_oupd( 5,0x02004DA);                // StopDisStart, StartOff1 = 100ns
_oupd( 6,0x0000000);
_oupd( 7,0x0281FB4);                // Res = 82.3045ps
_oupd(11,0x7FF0000);                // Any error -> ErrFlag
_oupd(12,0x4000000);                // Start# overflow to IrFlag
_oupd(14,0x0000000);
_oupd( 4,0x6400027);                // Master reset
StopDis1 = Low;                     // Enable inputs
StopDis2 = Low;
StopDis3 = Low;
StopDis4 = Low;
Wait(1µs);                          // Wait until Start01 is available from register 10
Sta01 = -inpd(10)& 0xFFFF           // read Sta01 = interval first int. Start - ext. Start
do
{
   if (EF1=Low)                                 // Data on IFIFO1?
   {
      data = _inpd(8);                          // Read IFIFO1
      Chan = (data & 0xC000000)>>26 + 1;        // Get channel#
      Start = (data & 0x3FC0000)>>18;           // Get Start#
      Time = (data & 0x1FFFF)-0x4DA;            // Get time Stop-Start
      if (Time<0)                               // Negative time refers to next start
      {
         Time = Time + 1µs;                     // Remap time to old start
         Start = Start -1                       // Correct start number
      }
      Printf(Chan,Start,Time);
   }
   if (EF2=Low)                                 // Data on IFIFO2?
   {
      data = _inpd(9);                          // Read IFIFO2
      Chan = ((data & 0xC000000)>>26) + 5;      // Get channel#
      Start = (data & 0x3FC0000)>>18;           // Get Start#
      Time = (data & 0x1FFFF)-0x4DA;            // Get time Stop-Start
      if (Time<0)                               // Negative time refers to next start
      {
         Time = Time + 1µs;                     // Remap time to old start
         Start = Start -1                       // Correct start number
      }
      Printf(Chan,Start,Time);
   }
} while(!quit)
```

3 G-Mode

3.1 Block diagram G-Mode

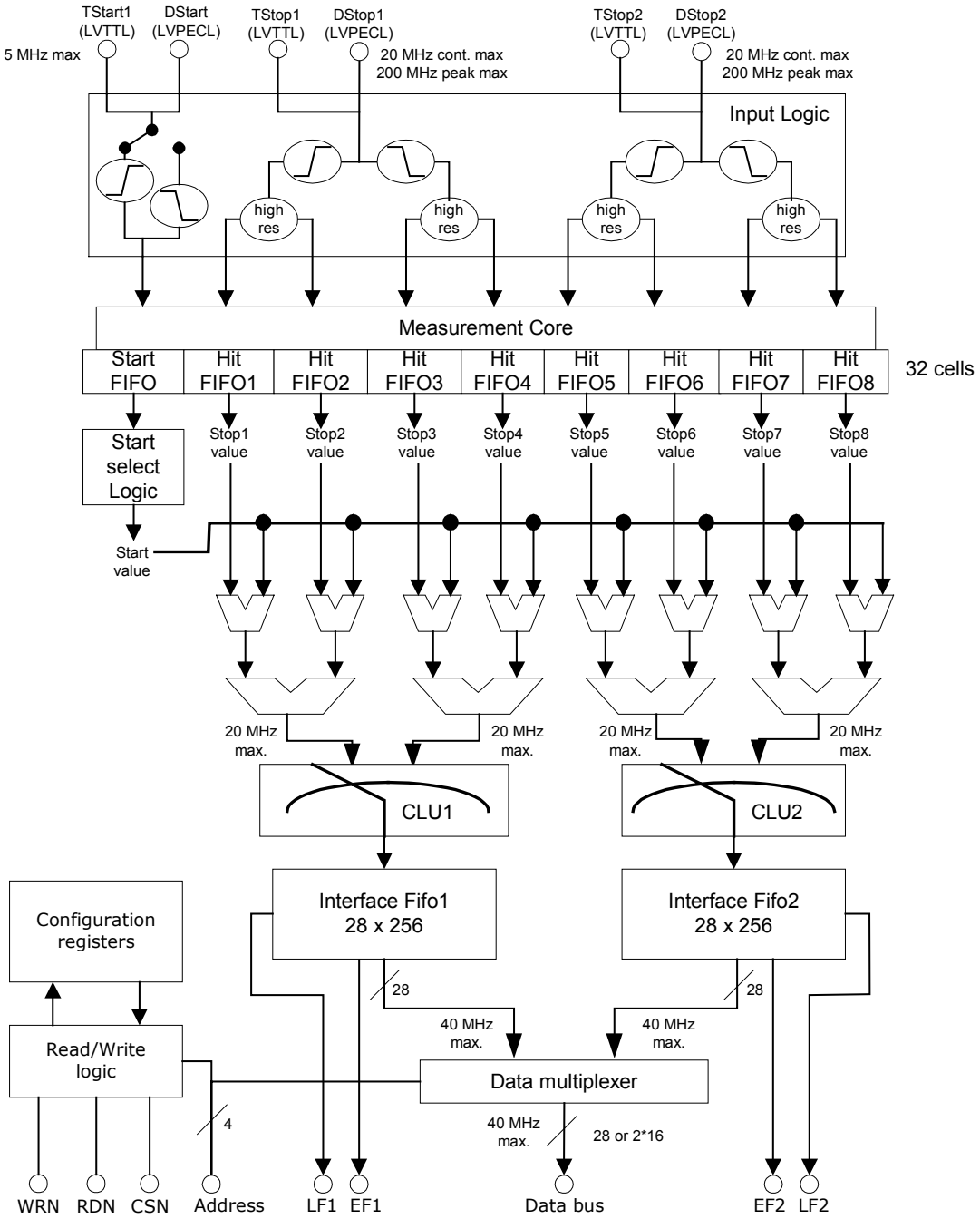


Figure 23

3.2 Input Circuitry G-Mode

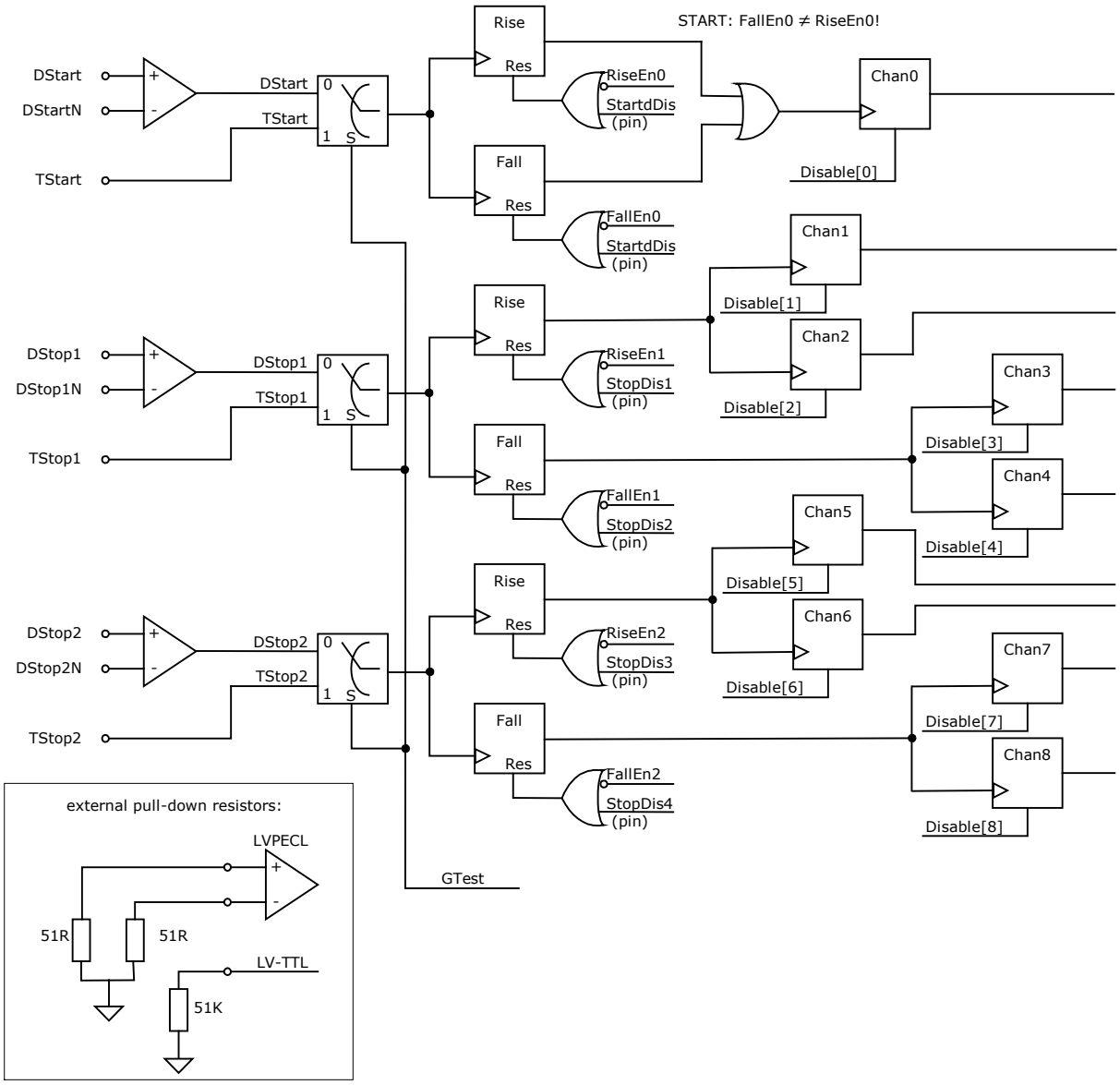


Figure 24

3.3 G-Mode Basics

In this mode the TDC-GPX offers:

- 2 Stop channels referring to 1 start channel
- Each of 36 ps resolution
- Rising and Falling edge for pulse width measurement down to 1.5ns
- Start-retrigger up to 5 MHz
- 4.7 ns pulse-pair resolution
- 0 to 65 µs measuring range
- Minimum 32-fold multihit capability
- Optional quiet mode
- LVPECL inputs

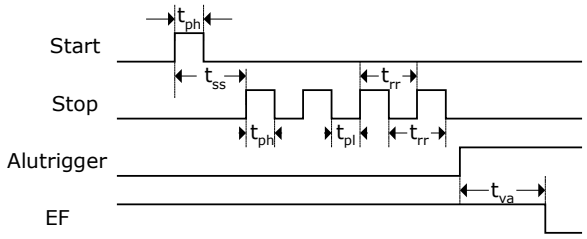


Figure 25. Measurement timings

Parameter	Time (Condition)	Description
t_{ph}	1.5 ns (min.)	Positive pulse width
t_{pl}	1.5 ns (min.)	Negative pulse width
t_{ss}	0 ns min *5.2 ns min 64 µs (max)	Start to Stop *with StopDisStart = 1
t_{rr}	5.5 ns (typ.)	Rising edge to rising edge
t_{ff}	5.5 ns (typ.)	Falling edge to falling edge
t_{va}	107 ns (max.)	ALU start to data valid

In this mode the TDC-GPX has two independent STOP input channels, each one capable of measuring the rising and falling edge at the same time. Each channel can store minimum 32 hits.

For improvement of the measurement accuracy, two channels are internally combined, which leads to a resolution of typical 40 ps. The paired channels are called combined channels. Each one of these combined channels measures rising or falling edges of one sampling channel. With this method it is possible to measure pulses with a pulse-width down to the minimum pulse-width allowed by the differential inputs, which is typ. 1.5 ns. Two adjacent rising or falling edges on a sampling channel may have a delay of down to 5.5 ns (typ.).

Each STOP input has an 8 Bit stop counter, sensitive to the falling edge. The number of hits for each input can be read from register 11, StopCounter0 and StopCounter1.

Internally the Start is shifted by an offset (in multiples of LSB). This allows measuring hits that arrive earlier than the start signal and to measure down to 0.

Input circuitry

In G-Mode the TDC-GPX has differential low-voltage PECL input buffers. The power for the differential inputs has to be switched on separately by setting register 6, PowerOnECL = '1'.

The detailed input structure is shown in Figure 24. Each input separately can be set to be sensitive to rising and/or falling edge. This is done in register0, RiseEn0..2 and FallEn0..2. A zero in both bits for one channel at the same time disables the channel.

All inputs can be disabled by hardware, the stop inputs separately for rising and falling edges (pin 'StopDis1' disables inputs DStop1, rising edge etc.).
They also can be disabled by software setting the 'Disable' in register 2. The 'Disable' bits have to be set in pairs, e.g Disable3 and Disable4 to disable Dstop, falling edge.

StopDisStart & StartDisStop

By default the Start and Stop inputs of the TDC-GPX are open immediately after a reset.

The consequence for the Stop channels is that even hits coming before a Start pulse will be measured. The bit StopDisStart in register 5 disables the Stop channels until there is a Start pulse. A consequence is that there is a minimum delay of 7 ns after the Start before hits are accepted on the Stop channels.

With single-start only the first Start pulse is used for the measurement. In case more than one Start pulse is expected this might cause an overflow of the Hit FIFO of the Start channel. This will produce garbage data. There we recommend setting the StartDisStart bit in register 5. A '1' disables the Start channel after the first Start pulse.

External Start Retrigger

A further option is to retrigger the Start externally. This option is activated by setting StartRetrig = 1 (Reg 5). The maximum retrigger frequency is limited to typically 5 MHz. Higher rates will disturb the chip.

Start-Offset
For several reasons a mathematical offset is added to the stop time. One reason is to compensate for different internal delays from the input buffers to the TDC unit in the Start and Stop paths. The other reason is to allo the ALU to look "into the past" without handling negative values (which the ALU could not do). It allows handling Start-Stop intervals down to 0 and even less. In G-Mode the TDC-GPX creates a second pulse on the Start channel by its own. Therefore two offset values have to be set. 'StartOff1' in register 5 and StartOff2 in register 6, both in multiples of BIN and 18 bits wide. Internally the start offset is added to the time measurement result and has to be subtracted from the value read from the TDC.

Adjusting the Start-Offset
The Start-Offset register of the TDC-GPX allows the compensation for the offset due to the different internal delays. It allows to do measurements down to 0 ns time intervals between Start and Stop. The correct setting should be done by experiment.

Procedure:
1. Set StartOff1 = StartOff2 = 0
2. Apply Start and Stop signals with a short delay (e.g. 12ns)
3. Step down the interval and look at the output data. They are getting smaller and smaller until you pass the first internal Start time stamp. The output data then jumps to a very high value.
4. Take the time interval t_{cross1} (from your generator) where this happens
5. Calculate StartOff1 = t_{cross1} / BIN and write this value into register 5, StartOff1
6. Continue stepping down the time interval until you see the same effect as in 3
7. Take the time interval t_{cross2} (from your generator) and calculate StartOff2 = t_{cross2} / BIN
8. Write this value into register 6

Internal Data Processing
The raw values of the stop events are stored in 32-stage Hit FIFOs. This Hit FIFO can be filled with data at a peak rate of 182 MHz.

The following pipelined post-processing unit is responsible for compression, Start selection and correct Stop-Start subtraction. Subsequently a collection unit transfers the data to the Interface FIFOs, which are 256 stages deep. Each channel has its own interface FIFO. The maximum rate for transfer into the Interface FIFO is 40 MHz, 20 MHz for rising edge data and 20 MHz for falling edge data.

Finally a data multiplexer adds data from both Interface FIFOs to the data bus. The data bus is 28 Bits wide and capable of 40 MHz transfer rate. The data bus can be switched to 16 Bit width writing 0x0000010 into address 14. A LOW at pin 'Output enable' forces the bidirectional bus drivers to permanent output state. This is helpful for fast data read out routines.
Each Interface FIFO has an empty flag (EF) and a load-level flag (LF). All flags are HIGH active. At low data rates it is recommended to check the EF to see whether there are data available for read out. It is not allowed to read from an empty Interface FIFO. The LF is helpful at high data rates. The load level threshold can be set in 'Fill' in register 6 and is the same for both FIFOs. As soon as the set number of data is available this can be read from the FIFO as a block without the need of checking the EF.
Note: the load-level flags are not synchronized. The load-level flag for a FIFO is valid only if it is **not** read from this FIFO. Otherwise there might be spikes.

Quiet Mode
TDC-GPX offers two options for the post-processing:

- Quiet Mode
- Non-quiet Mode

In Quiet Mode the post-processing and calculation does not start automatically after each single event, but after a dedicated trigger. The trigger can be given externally by a rising slope at pin ALUTRIGGER or by software setting a dedicated ALU-Trigger Bit. This mode is introduced to reduce the noise during a measurement and to allow the small values for pulse-pair and pulse-width resolution.

In the Non-quiet Mode, the post-processing starts immediately after the first hit arrived in a raw FIFO. The post-processing doesn't start before there is a START signal and at least one STOP signal.
The time needed from the start of the post-processing until first data is available in the interface FIFO is typ. 200 ns.

3.4 Data structure and readout

The output data are integers with a LSB width defined by the setting of the resolution adjust unit.

$$BIN = \frac{T_{ref} \times 2^{refclkdiv}}{216 \times hsdiv} \times \frac{1}{2}$$

Bit22	Bit21..0
1=rising edge 0=falling edge	Edge-to-Start result of the addressed combined channel

The data can be read from address 8 for interface FIFO1 (DStop1) and from address 9 for interface FIFO2 (DStop2).

3.5 Reset

There are 3 ways of resetting the device:

- **Power-up reset**: a low signal at pin PURESN resets the whole chip.
- **Master-Reset**: this command resets everything except the configuration registers. It can be done by software writing to register 4. In non-quiet mode MasterAluTrig in register 5 can be set to '1'. Then this command can be done also by a HIGH at the Alutrigger input pin. In quiet mode MasterOenTrig in register 5 can be set to '1'. Then this command can be done also by a LOW at the OEN input pin (only with OEN off).
- **Partial-Reset**: this command resets everything except the configuration registers and the Interface FIFOs. It can be done by software writing to register 4. In non-quiet mode Partial-AluTrig in register 5 can be set to '1'. Then this command can be done also by a HIGH at the Alutrigger input pin. In quiet mode PartialOenTrig in register 5 can be set to '1'. Then this command can be done also by a LOW at the OEN input pin (only with OEN off).

After a Power-on reset or a Master reset it takes 40 ns before the Start and Stop inputs accept data.
After a Partial reset it takes 75 ns before the Start and Stop inputs accept data.

3.6 MTimer

There is an internal timer available for internal use. The main application will be setting a dedicated time interval between 25ns and 204.7 µs after which the interrupt flag is set. The period is set in 'MTimer', register 7, in multiples of Tref. The maximum delay is 8191 * Tref = 204.7 µs. The timer can be started by a Stop and/or Start signal. This is set in 'MTimerStart' and 'MTimerStop', register 4. Setting Bit 'TimerFlag', register 12, the interrupt flag is set when the timer stops.

3.7 Interrupt Flag

The user can select on which event(s) the interrupt flag is set.
The selection is done in register 12, Bits 13 to 25, by unmasking the dedicated bits. They are combined by an Or-Gate to the interrupt flag.
Selectable events are

- Hit FIFOs 1, 2 ...or/and 8 are full
- Interface FIFOs 1 or/and 2 are full
- PLL not locked
- All Hit FIFOs empty
- End of Mtimer

3.8 Error Flag

The user can select on which event(s) the error flag is set.
The selection is done in register 11, Bits 16 to 26, by unmasking the dedicated bits. They are combined by an Or-Gate to the error flag.
Selectable events are

- Hit FIFOs 1, 2 ...or/and 8 are full
- Interface FIFOs 1, 2 ...or/and 8 are full
- PLL not locked

3.9 Testinputs

For test purpose a set of three TTL inputs can be multiplexed to the measuring circuit by setting Bit Gtest in register 3. The test inputs have the same functionality as the measure inputs, but can only handle a minimum pulse width of 5ns and a minimum edge-to-edge distance of 20ns.

3.10 RaSpeed & DelX

The on-chip timings for measuring rising and falling edge down to 1.5 ns are very critical. For some chips it might be necessary to add an internal, additional delay to guarantee correct data processing. These delays are set by the RaSpeed bits and the DelRisex/DelFallx/DelTx in registers 2, 3 and 4. Increasing those will reduce the pulse-pair resolution of the TDC-GPX .

RaSpeed & DelX	Pulse-pair resolution
0	5.5 ns
1	6.5 ns
2	7.5 ns
3	8.5 ns

3.11 G-Mode Timing & Resolution

The delay parameters vary with voltage, temperature and process tolerance. The following table lists the derating factors.

Derating by	Minimal	Maximal
Voltage	0.91 at 3.6V	1.2 at 2.85V
Temperature	0.889 at -40°C	1.17 at +125°C
Process	0.74 at BC	1.31 at WC

With the stabilization of the resolution by the resolution adjust mode, the voltage of the core decreases with decreasing temperature, and increases with increasing temperature. The setting should be done in a way that at maximum operating temperature the maximum core voltage is reached, and that minimum core voltage is reached at minimum operating temperature. With this method you get two limits:

Best case process, deepest temperature, lowest voltage: 0.74 x 0.889 x 1.2 = 0.789
Worst case process, highest temperature, highest voltage: 1.31 x 1.17 x 0.91 = 1.394

With a typical resolution of 40ps (typ. process, 25°C, 3.3V) you get two limits for the resolution:

	Best	Worst
Resolution (of combined channels)	32 ps	56 ps

The BIN or LSB width is defined by the setting of the resolution adjust unit (1.6.1 Resolution adjust),
The standard deviation (1 σ) of the result is typically 1 LSB + 4 ps * Δt/µs.

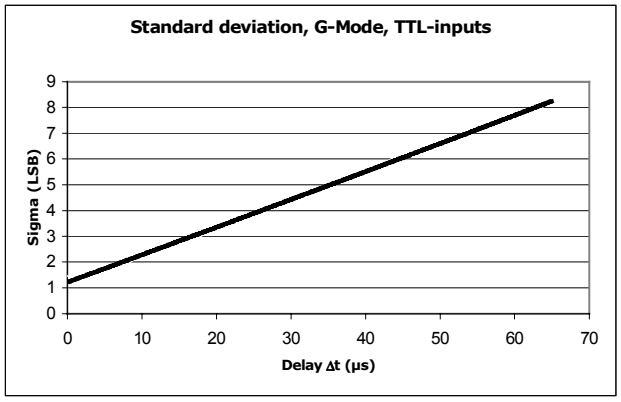


Figure 26

DNL

the TDC-GPX shows a moderate differential non-linearity (DNL) because internal propagation delays were used for the time measurement and because those delays are different for rising and falling edges, but the variation from channel to channel is systematic. The following diagram shows the DNL data at a resolution of 37 ps:

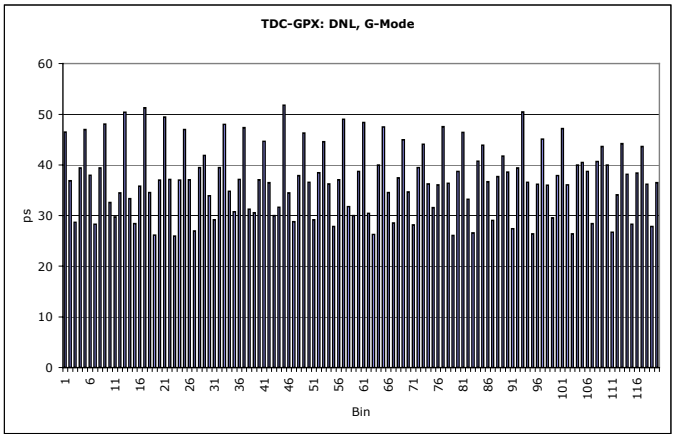


Figure 27

3.12 Measurement Flow

In the following we shows a typical example of register settings and measurement flow in G-Mode.

Task: Typical application laser rangefinder
Measuring Stops on 2 channels, rising and falling edge, within a window of 1 µs from Start.

```
//****** G-Mode, Stops against single Start **********

PuResN=Low;                         // Power-up reset
PuResN=High;

StopDis1 = High;                    // Disable inputs
StopDis2 = High;
StopDis3 = High;
StopDis4 = High;
                                    // write configuration registers:
_oupd( 0,0x00000FF);                // Rising and falling edges, Start ringoscil.
_oupd( 1,0x5050500);                // Channel adjust = 5 for each second stop channel
_oupd( 2,0x0050001);                // G-Mode, channel adjust = 5
_oupd( 3,0x0000000);                // Use differential inputs
_oupd( 4,0x6000000);                // Mtimes trig. by Start, EFlagHiZN
_oupd( 5,0x0E00080);        //StopDisStart, StartDisStart, StartOff1 = 10ns, MasterAluTrig
_oupd( 6,0x0100000);                // StartOff2 = 20ns
_oupd( 7,0x0141FB4);                // Res = 41.1523ps, Mtimer = 1µs
_oupd(11,0x7FF0000);                // Any error -> ErrFlag
_oupd(12,0x2000000);                // Mtimer -> IrFlag
_oupd(14,0x0000000);

_oupd( 4,0x6400000);                // Master reset

StopDis1 = Low;                     // Enable inputs
StopDis2 = Low;
StopDis3 = Low;
StopDis4 = Low;

do
{
   while(IrFlag=Low);                           // Check interrupt flag

   while((EF1=Low)or(EF2=Low))                  // Check empty flag
   {
      if (EF1=Low)                              // Data on IFIFO1?
      {
         data = _inpd(8);                       // Read IFIFO1
         Chan = 1;                              // Channel#
         Edge = ((data & 0x0400000)>>26) + 1;   // Get edge
         Time = (data & 0x3FFFFF);              // Get time Stop-Start
         Printf(Chan,Edge,Time);
      }
      if (EF2=Low)                              // Data on IFIFO2?
      {
         data = _inpd(9);                       // Read IFIFO2
         Chan = 2;                              // Channel#
         Edge = ((data & 0x0400000)>>26) + 5;   // Get edge
         Time = (data & 0x3FFFFF);              // Get time Stop-Start
         Printf(Chan,Edge,Time);
      }
   }
   Alutrigger = High;                           // Master reset
   Alutrigger = Low;
} while(!quit)
```

4 R-Mode

4.1 Block diagram R-Mode

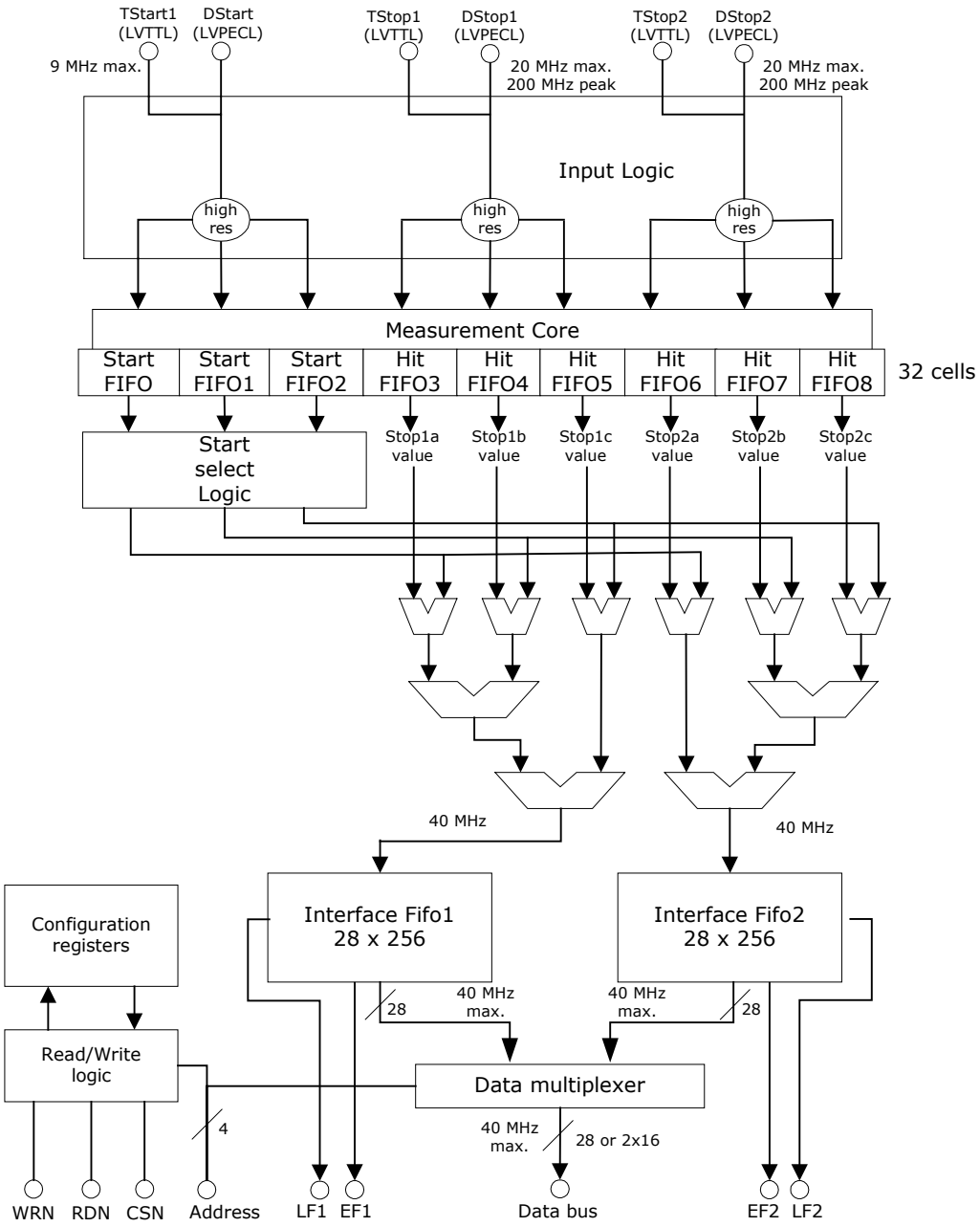


Figure 28

4.2 Input Circuitry R-Mode

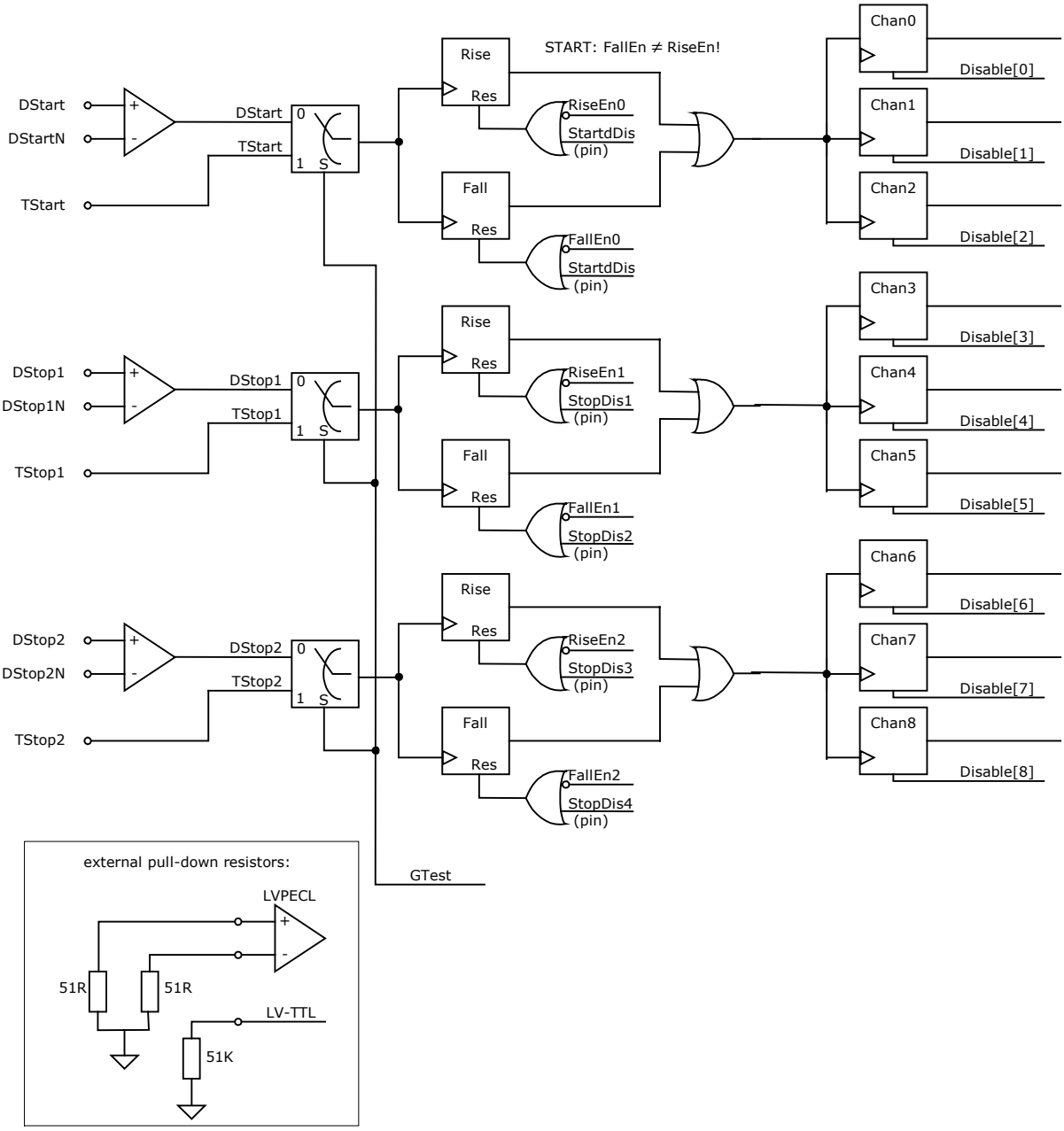


Figure 29

4.3 R-Mode Basics

In this mode the TDC-GPX offers:

- 2 Stop channels referring to 1 start channel
- Each of 27 ps resolution
- Start-retrigger up to 9 MHz
- Rising or falling edge
- 5.5 ns pulse-pair resolution
- 0 to 40 µs measuring range
- Minimum 32-fold multihit capability
- Optional quiet mode
- LVPECL inputs

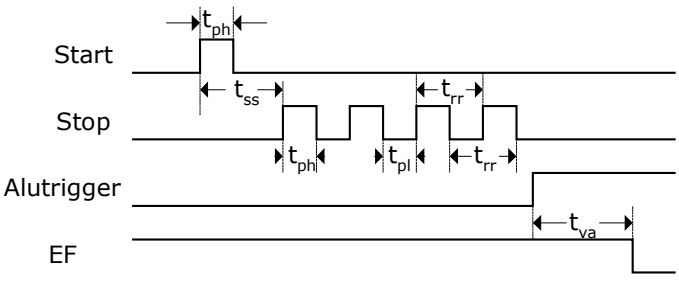


Figure 30 Measurement timings

Parameter	Time (Condition)	Description
t_{ph}	1.5 ns (min.)	Minimum pulse width
t_{pl}	1.5 ns (min.)	Minimum pulse width
t_{ss}	0 ns (min) *5.2 ns (min) 40 µs (max.)	Start to Stop *with StopDisStart = 1
t_{rr}	5.5 ns (typ.)	Rising edge to rising edge
t_{ff}	5.5 ns (typ.)	Falling edge to falling edge
t_{va}	107 ns (max.)	ALU start to data valid

In this mode the TDC-GPX has two independent STOP input channels, each one capable of measuring the rising or falling. Each channel can store a minimum of 32 hits.

For improvement of the measurement accuracy, three channels are internally combined, which leads to a resolution of typical 27 ps. The trebled channels are called combined channels. Each one of these combined channels measures rising or falling edges of one sampling channel. Two adjacent rising or falling edges on a sampling channel may have a delay of down to 5.5 ns (typ.).
Each STOP input has an 8 Bit stop counter, sensitive to the rising edge. The number of hits for each input can be read from register 11, StopCounter0 and StopCounter1.

Internally the Start is shifted by an offset (in multiples of LSB). This allows measuring hits that arrive earlier than the start signal and to measure down to 0 ns.

Input circuitry
In R-Mode the TDC-GPX has differential low-voltage PECL input buffers. The power for the differential inputs has to be switched on separately by setting register 6, PowerOnECL = '1'.

The detailed input structure is shown in Figure 29. Each input can be set to be sensitive to rising or falling edge. This is done in register0, RiseEn0..2 and FallEn0..2. A zero in both bits for one channel at the same time disables the channel.

All inputs can be disabled by hardware, the stop inputs separately for rising and falling edges (pin 'StopDis1' disables inputs DStop1,rising edge etc.).
They also can be disabled by software setting the 'Disable' in register 2. The 'Disable' bits have to be set in triples, e.g Disable3, Disable4 and Disable5 to disable DStop1.

StopDisStart & StartDisStop
By default the Start and Stop inputs of the TDC-GPX are open immediately after a reset.

The consequence for the Stop channels is that even hits coming before a Start pulse will be measured. The bit StopDisStart in register 5 disables the Stop channels until there is a Start pulse. A consequence is that there is a minimum delay of 7 ns after the Start before hits are accepted on the Stop channels.

With single-start only the first Start pulse is used for the measurement. In case more than one Start pulse is expected this might cause an overflow of the Hit FIFO of the Start channel. This will produce garbage data. There we recommend setting the StartDisStart bit in register 5. A '1' disables the Start channel after the first Start pulse.

External Start Retrigger
A further option is to retrigger the Start externally. This option is activated by setting StartRetrig = 1 (Reg 5). The maximum retrigger frequency is limited to typically 9 MHz. Higher rates will disturb the chip.
Start-Offset

For several reasons a programmable offset is added to the stop time. One reason is to compensate for different internal delays from the input buffers to the TDC unit in the Start and Stop paths. The other reason is to allo the ALU to look "into the past" without handling negative values (which the ALU could not do). It allows handling Start-Stop intervals down to 0 and even less. The offset value 'StartOff1' is set in register 5 in multiples of 3 x BIN and 18 bits wide. Internally the start offset is added to the time measurement result and has to be subtracted from the value read from the TDC.

Adjusting the Start-Offset

The Start-Offset register of the TDC-GPX allows the compensation for the offset due to the different internal delays. It allows to do measurements down to 0 ns time intervals between Start and Stop. The correct setting should be done by experiment.

Procedure for single start applications:

1. Set StartOff1 = 0
2. Apply Start and Stop signals with a short delay (e.g. 12ns)
3. Step down the interval and look at the output data. They are getting smaller and smaller until you pass the internal Start time stamp. The output data then jumps to a very high value.
4. Take the time interval t_{cross} (from your generator) where this happens
5. Calculate StartOff1 = t_{cross} / 3 x BIN and write this value into register 5, StartOff1. In case you expect negative values add an additional amount X to StartOff1 and substract this value later on from your output data

With start retrigger the value StartOff1 should be set to

StartOff1 = 1,000 (≈ 81 ns).

The reason is that the ALU is internally stopped for about 50 ns during a start retrigger to add the new start time stamp. If there is a hit during this period the ALU will need
25 ns + 50 ns = 75 ns to transfer those data to the IFIFO. The ALU cannot handle negative values. Therefore the start offset is added so that the ALU can handle the data being collected during the break. In case the input data rate is higher (bursts) it might be necessary to increase also the offset value , e.g. to 10,000.
The start retrigger adds some indeterminacy – due to the 25ns reference – to whether a stop refers to the old start or the new one. This is not an uncertainty.

Each time stamp that is negative after offset substraction can be remapped to the old start by adding the start period.

Internal Data Processing

The raw values of the stop events are stored in 32-stage Hit FIFOs. This Hit FIFO can be filled with data at a peak rate of 182 MHz.
The following pipelined post-processing unit is responsible for compression, Start selection and correct Stop-Start subtraction. Subsequently a collection unit transfers the data to the Interface FIFOs, which are 256 stages deep. Each channel has its own interface FIFO. The maximum rate for transfer into the Interface FIFO is 40 MHz.

Finally a data multiplexer adds data from both Interface FIFOs to the data bus. The data bus is 28 Bits wide and capable of 40 MHz transfer rate. The data bus can be switched to 16 Bit width writing 0x0000010 into address 14. A LOW at pin 'Output enable' forces the bidirectional bus drivers to permanent output state. This is helpful for fast data read out routines.
Each Interface FIFO has an empty flag (EF) and a load-level flag (LF). All flags are HIGH active. At low data rates it is recommended to check the EF to see whether there are data available for read out. It is not allowed to read from an empty Interface FIFO. The LF is helpful at high data rates. The load level threshold can be set in 'Fill' in register 6 and is the same for both FIFOs. As soon as the set number of data is available this can be read from the FIFO as a block without the need of checking the EF.

Note: the load-level flags are not synchronized. The load-level flag for a FIFO is valid only if it is **not** read from this FIFO. Otherwise there might be spikes.

Quiet Mode

TDC-GPX offers two options for the post-processing:

- Quiet Mode
- Non-quiet Mode

In Quiet Mode the post-processing and calculation does not start automatically after each single event, but after a dedicated trigger. The trigger can be given externally by a rising slope at pin ALUTRIGGER or by software setting a dedicated ALU-Trigger Bit. This mode is introduced to reduce the noise during a measurement and to allow the small values for pulse-pair and pulse-width resolution.

In the Non-quiet Mode, the post-processing starts immediately after the first hit arrived in a raw FIFO. The post-processing doesn't start before there is a START signal and at least one STOP signal.
The time needed from the start of the post-processing until first data is available in the interface FIFO is typ. 200 ns.

4.4 Data structure and readout

The output results are integers with a LSB width defined by the setting of the resolution adjust unit.

$$BIN = \frac{T_{ref} \times 2^{refclkdiv}}{216 \times hsdiv} \times \frac{1}{3}$$

Bit 27 … 23	Bit 22...0
Not used	Edge-to-Start result of the addressed combined channel

The data can be read from address 8 for interface FIFO1 and from address 9 for interface FIFO2.

4.5 Reset

There are 3 ways of resetting the device:

- **Power-up reset**: a low signal at pin PURESN resets the whole chip.
- **Master-Reset**: this command resets everything except the configuration registers. It can be done by software writing to register 4. In non-quiet mode MasterAluTrig in register 5 can be set to '1'. Then this command can be done also by a HIGH at the Alutrigger input pin. In quiet mode MasterOenTrig in register 5 can be set to '1'. Then this command can be done also by a LOW at the OEN input pin (only with OEN off).
- **Partial-Reset**: this command resets everything except the configuration registers and the Interface FIFOs. It can be done by software writing to register 4. In non-quiet mode Partial-AluTrig in register 5 can be set to '1'. Then this command can be done also by a HIGH at the Alutrigger input pin. In quiet mode PartialOenTrig in register 5 can be set to '1'. Then this command can be done also by a LOW at the OEN input pin (only with OEN off).

After a Power-on reset or a Master reset it takes 40 ns before the Start and Stop inputs accept data.
After a Partial reset it takes 75 ns before the Start and Stop inputs accept data.

4.6 MTimer

There is an internal timer available for internal use. The main application will be setting a dedicated time interval between 25ns and 204.7 µs after which the interrupt flag is set. The period is set in 'MTimer', register 7, in multiples of Tref. The maximum delay is 8191 * Tref = 204.7 µs. The timer can be started by a Stop and/or Start signal. This is set in 'MTimerStart' and 'MTimerStop', register 4. Setting Bit 'TimerFlag', register 12, the interrupt flag is set when the timer stops.

4.7 Interrupt Flag

The user can select on which event(s) the interrupt flag is set.
The selection is done in register 12, Bits 13 to 25, by unmasking the dedicated bits. They are combined by an Or-Gate to the interrupt flag.
Selectable events are

- Hit FIFOs 1, 2 …or/and 8 are full
- Interface FIFOs 1 or/and 2 are full
- PLL not locked
- All Hit FIFOs empty
- End of Mtimer

4.8 Error Flag

The user can select on which event(s) the error flag is set.
The selection is done in register 11, Bits 16 to 26, by unmasking the dedicated bits. They are combined by an Or-Gate to the error flag.
Selectable events are

- Hit FIFOs 1, 2 …or/and 8 are full
- Interface FIFOs 1, 2 …or/and 8 are full
- PLL not locked

4.9 Testinputs

For test purpose a set of three TTL inputs can be multiplexed to the measuring circuit by setting Bit Gtest in register 3. The test inputs have the same functionality as the measure inputs, but can only handle a minimum pulse width of 5ns and a minimum edge-to-edge distance of 20ns.

4.10 RaSpeed & Delx

The on-chip timings for measuring rising and falling edge down to 1.5 ns are very critical. For some chips it might be necessary to add an internal, additional delay to guarantee correct data processing. These delays are set by the RaSpeed bits and the DelRisex/DelFallx/DelTx in registers 2, 3 and 4. Increasing those will reduce the pulse-pair resolution of the TDC-GPX .

RaSpeed & Delx	Pulse-pair resolution
1	5.5 ns
2	6.5 ns
3	7.5 ns

4	8.5 ns

The on-chip timings for measuring rising and falling edge down to 1.5 ns are very critical. For some chips it might be necessary to add an internal, additional delay to guarantee correct data processing. These delays are set by the RaSpeed bits and the DelRisex/DelFallx/DelTx in registers 2, 3 and 4. Increasing those will reduce the pulse-pair resolution of the TDC-GPX .

RaSpeed & Delx	Pulse-pair resolution
0	5.5 ns
1	6.5 ns
2	7.5 ns
3	8.5 ns

4.11 R-Mode Timing & Resolution

TDC-GPX is working in resolution adjust mode. The resolution adjust unit is identical with TDC-F1's unit. The delay parameters vary with voltage, temperature and process tolerance. The following table lists the derating factors.

Derating by	Minimal	Maximal
Voltage	0.91 at 3.6V	1.2 at 2.85V
Temperature	0.889 at –40°C	1.17 at +125°C
Process	0.74	1.31

With the stabilization of the resolution by the resolution adjust mode, the voltage of the core decreases with decreasing temperature, and increases with increasing temperature. The setting should be done in a way that at maximum operating temperature the maximum core voltage is reached, and that minimum core voltage is reached at minimum operating temperature. With this method you get two limits:

Best case process, deepest temperature, lowest voltage: 0.74 x 0.889 x 1.2 = 0.789
Worst case process, highest temperature, highest voltage: 1.31 x 1.17 x 0.91 = 1.394

From validation measurement the typical BIN size has been 27 ps (typ. process, 25°C, 3.3V). With the above-mentioned derating factors this gives two limits for the resolution:

	Best	Worst
Resolution	21 ps	38 ps

The BIN or LSB width is defined by the setting of the resolution adjust unit (1.6.1 Resolution adjust),

The standard deviation (1 σ) of the result is typically 1.4 LSB + 2,8 ps * Δt/µs.

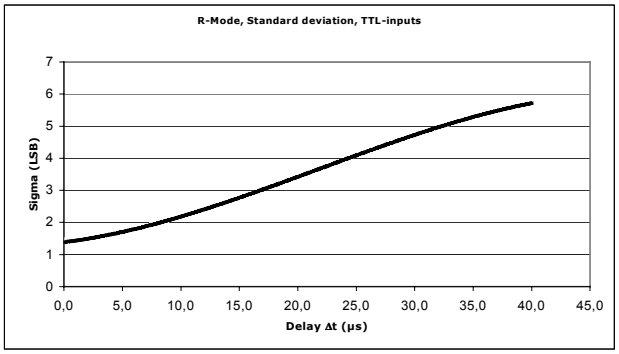


Figure 31

The pulse width limit is 1.5 ns typically, limited by the input buffers.

The measurement range depends on the bin size and the coarse counter. Its typical value is:
Measurement range = 54 x 32767 x 27 ps
= 47 µs

DNL

The TDC-GPX shows a moderate differential non-linearity (DNL) because internal propagation delays were used for the time measurement and because those delays are different for rising and falling edges, but the variation from channel to channel is systematic. The following diagram shows the DNL data at a resolution of 27 ps:

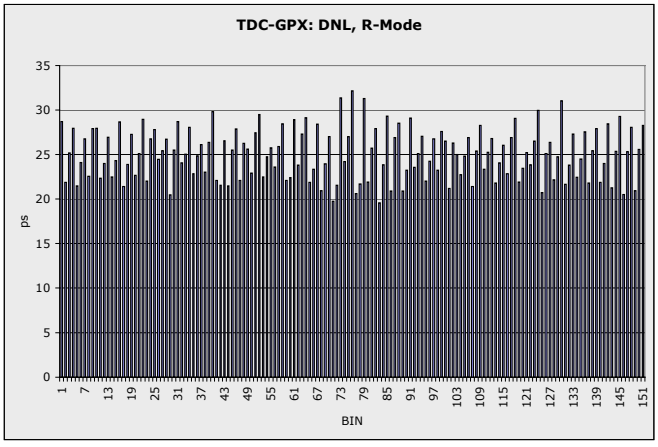


Figure 32

4.12 Measurement Flow

In the following we shows a typical example of register settings and measurement flow in R-Mode.

Task1: Typical application spectroscopy or testing.
Given a Start signal with 1 MHz rate. To each Start there is one Stop event on channel 1. The time between Stop and Start shall be measured with high resolution, using the LVTTL inputs.
Choice: R-Mode with Start retrigger, using the Fill level flags.

```
//****** R-Mode, Stop against Start **********

PuResN=Low;                         // Power-up reset
PuResN=High;

StopDis1 = High;                    // Disable inputs
StopDis2 = High;
StopDis3 = High;
StopDis4 = High;
                                    // write configuration registers:
_oupd( 0,0x000009F);                // Rising and falling edges, Start ringoscil.
_oupd( 1,0x0620620);                // Channel adjust = 6 & 2
_oupd( 2,0x0062004);                // R-Mode, channel adjust = 6 & 2
_oupd( 3,0x8000000);                // Use LVTTL inpus
_oupd( 4,0x2000000);                // EFlagHiZN
_oupd( 5,0x80004DA);                // StartOff1 = 100ns, StartRetrigger
_oupd( 6,0x00000C8);                // Fill = 200
_oupd( 7,0x0001FB4);                // Res = 27.4348ps
_oupd(11,0x7FF0000);                // Any error -> ErrFlag
_oupd(12,0x0000000);                // No IrFlag
_oupd(14,0x0000000);

_oupd( 4,0x2400001);                // Master reset

StopDis1 = Low;                     // Enable inputs
StopDis2 = Low;
StopDis3 = Low;
StopDis4 = Low;

do
{
   if (LF1=High)                          // Fill level=200 IFIFO1 reached?
   {
      for (i=0;i<200,I++)                 // Read 200 times
      {
         data = _inpd(8);                 // Read IFIFO1
         Time = (data & 0x7FFFFF)-0x4DA;  // Get time Stop-Start
         Printf(Time);
      }
   }
} while(!quit)
```

Task2: Typical application laser rangefinder
Given a Start signal with 10 kHz rate. To each Start there is an unknown number of Stops on channel 1. The maximum range is 1 µs. The time between Stop and Start shall be measured with very high resolution, using the LVPECL inputs.
Choice: R-Mode with quiet mode and internal Timer.

```
//****** R-Mode, Stop against Start **********

PuResN=Low;                         // Power-up reset
```

```
PuResN=High;

StopDis1 = High;                    // Disable inputs
StopDis2 = High;
StopDis3 = High;
StopDis4 = High;
                                    // write configuration registers:
_oupd( 0,0x000009F);                // Rising and falling edges, Start ringoscil.
_oupd( 1,0x0620620);                // Channel adjust = 6 & 2
_oupd( 2,0x0062004);                // G-Mode, channel adjust = 6 & 2
_oupd( 3,0x0000000);                // Use LVPECL inpus
_oupd( 4,0x6000100);                // EFlagHiZN, Quiet mode, Mtimer on Start
_oupd( 5,0x00004DA);                // StartOff1 = 100ns
_oupd( 6,0x8000000);                // Power-on ECL
_oupd( 7,0x0141FB4);                // Res = 27.4348ps, Mtimer = 1 µs
_oupd(11,0x7FF0000);                // Any error -> ErrFlag
_oupd(12,0x2000000);                // Mtimer -> Interrupt flag
_oupd(14,0x0000000);

_oupd( 4,0x6400100);                // Master reset

StopDis1 = Low;                     // Enable inputs
StopDis2 = Low;
StopDis3 = Low;
StopDis4 = Low;

do
{
   while(IrFlag=Low);                           // Check interrupt flag

   Alutrigger = High;                           // Trigger Alu
   Alutrigger = Low;

   wait(100ns);                                 // Time to calculate first hit

   while(EF1=Low)                               // Check empty flag
   {
        data = _inpd(8);                        // Read IFIFO1
        Time = (data & 0x7FFFFF);               // Get time Stop-Start
        Printf(Time);
   }
   _oupd( 4,0x6400100);                         // Master reset
} while(!quit)
```

5 M-Mode

5.1 Block diagram M-Mode

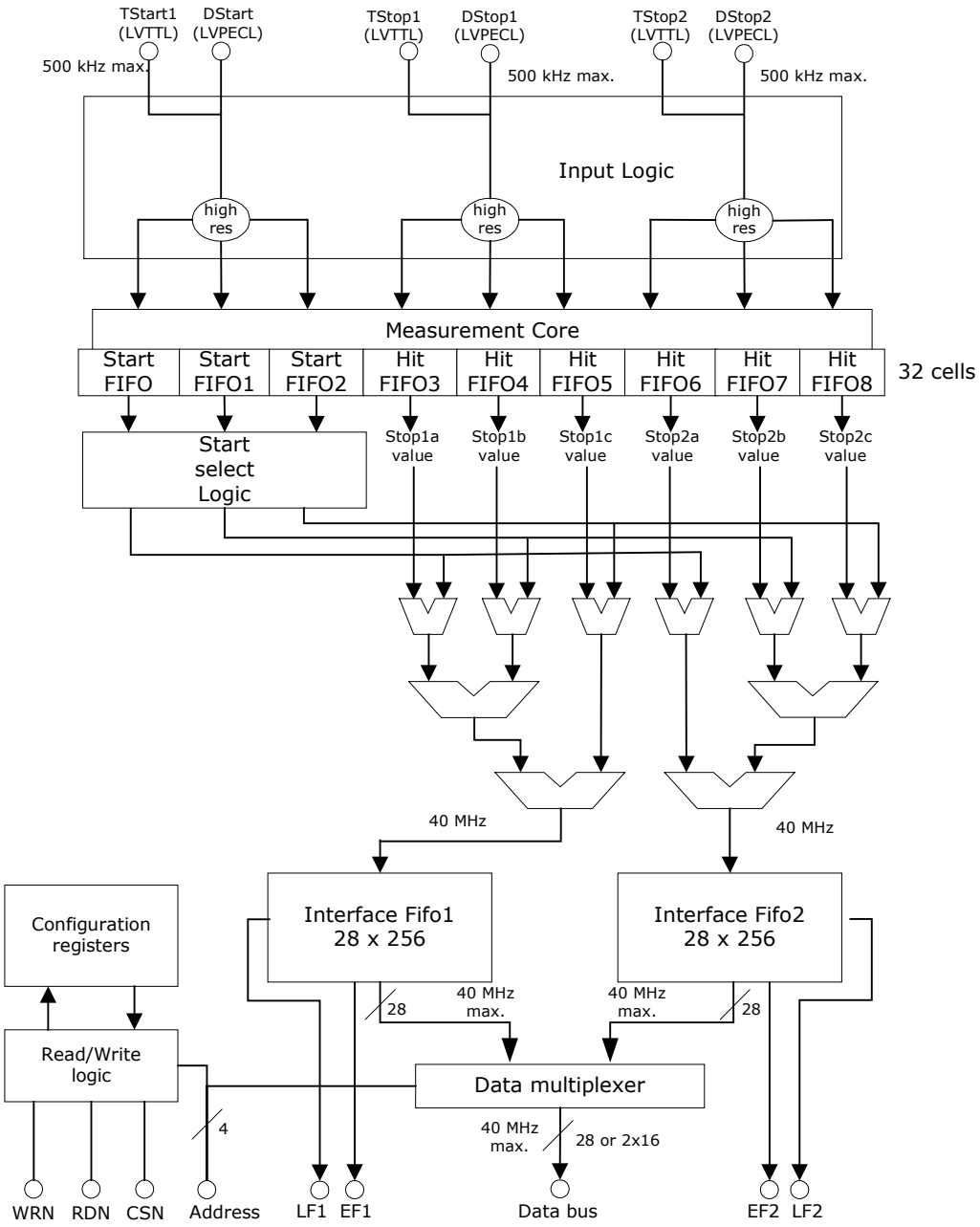


Figure 33

5.2 Input Circuitry M-Mode

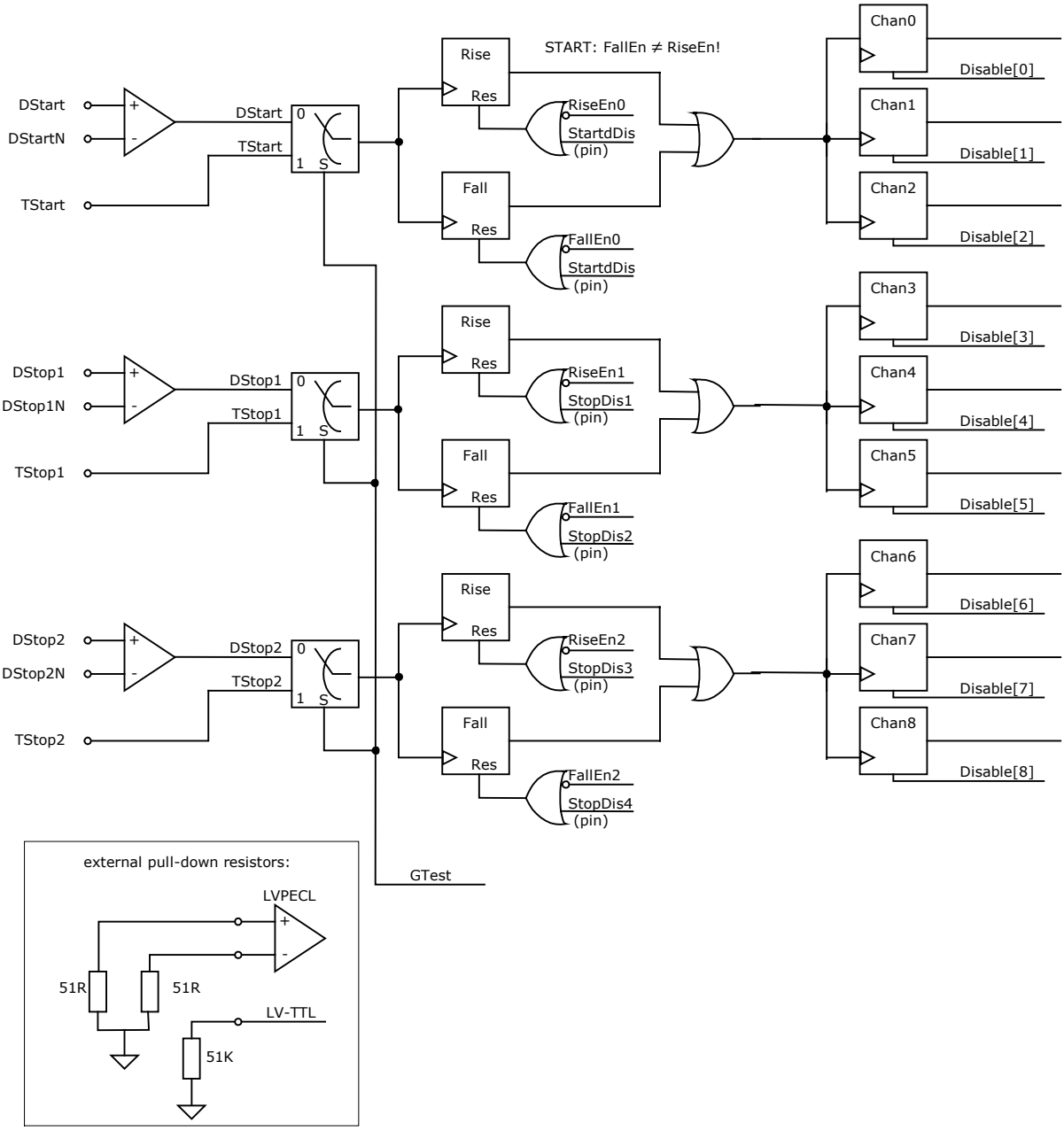


Figure 34

5.3 M-Mode Basics

- Maximum resolution:
  - Standard deviation down to 10 ps,
  - Peak-peak down to 70 ps
- 2 stop-channels referring to 1 start channel
- 1 Hit per channel
- 0 ns to 40 µs measuring range
- Quiet mode
- LVPECL inputs
- Max. 500 kHz continuous rate per channel
- Max. 1 MHz continuous rate per chip

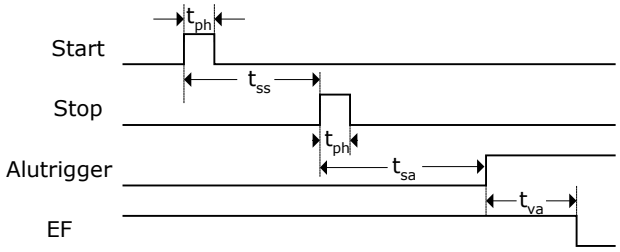


Figure 35: Measurement timings

Parameter	Time (Condition)	Description
t_{ph}	1.5 ns (min.)	Minimum pulse width
t_{pl}	3.2 ns (min.)	Minimum pulse width
t_{ss}	0 ns (min) 40 µs (max.)	Start to Stop
t_{sa}	400 ns (min)	Stop to ALU trigger
t_{va}	1 µs (max.)	ALU trigger to data valid

M-Mode is activated by setting MSet = 31 (Reg3) and Mon = 1 (Reg4).

The M-Mode for maximum resolution is basically an extension of the R-Mode. The block diagram and the input circuitry are the same as in R-Mode. Also the furhter settings are the same as in R-Mode.

In this mode the TDC-GPX accepts only one Stop per channel. It is necessary to select M-Mode in combination with quiet mode.

Input circuitry
In M-Mode the TDC-GPX has differential low-voltage PECL input buffers. The power for the differential inputs has to be switched on separately by setting register 6, PowerOnECL = '1'.

The detailed input structure is shown in Figure 29. Each input can be set to be sensitive to rising or falling edge. This is done in register0, RiseEn0..2 and FallEn0..2. A zero in both bits for one channel at the same time disables the channel.

All inputs can be disabled by hardware, the stop inputs separately for rising and falling edges (pin 'StopDis1' disables inputs DStop1,rising edge etc.).
They also can be disabled by software setting the 'Disable' in register 2. The 'Disable' bits have to be set in triples, e.g Disable3, Disable4 and Disable5 to disable DStop1.

StopDisStart & StartDisStop
By default the Start and Stop inputs of the TDC-GPX are open immediately after a reset.

The consequence for the Stop channels is that even hits coming before a Start pulse will be measured. The bit StopDisStart in register 5 disables the Stop channels until there is a Start pulse. A consequence is that there is a minimum delay of 7 ns after the Start before hits are accepted on the Stop channels.

With single-start only the first Start pulse is used for the measurement. In case more than one Start pulse is expected this might cause an overflow of the Hit FIFO of the Start channel. This will produce garbage data. There we recommend setting the StartDisStart bit in register 5. A '1' disables the Start channel after the first Start pulse.

Start-Offset
For several reasons a programmable offset is added to the stop time. One reason is to compensate for different internal delays from the input buffers to the TDC unit in the Start and Stop paths. It allows handling Start-Stop intervals down to 0 and even less. The offset value 'StartOff1' is set in register 5 in multiples of the I-Mode BIN and 18 bits wide. Internally the start offset is added to the time measurement result and has to be subtracted from the value read from the TDC.

Adjusting the Start-Offset
The Start-Offset register of the TDC-GPX allows the compensation for the offset due to the different internal delays. It allows to do measurements down to 0 ns time intervals between Start and Stop. The correct setting should be done by experiment.

Procedure for single start applications:
1. Set StartOff1 = 0

2. Apply Start and Stop signals with a short delay (e.g. 12ns)
3. Step down the interval and look at the output data. They are getting smaller and smaller until you pass the internal Start time stamp. The output data then jumps to a very high value.
4. Take the time interval t_{cross} (from your generator) where this happens
5. Calculate StartOff1 = t_{cross} / BIN and write this value into register 5, StartOff1. In case you expect negative values add an additional amount X to StartOff1 and substract this value later on from your output data

Internal Data Processing
The raw values of the stop events are stored in the Hit FIFOs.

The following pipelined post-processing unit is responsible for compression, Start selection and correct Stop-Start subtraction. Subsequently a collection unit transfers the data to the Interface FIFOs. Each channel has its own interface FIFO. The maximum rate for transfer into the Interface FIFO is 40 MHz.

Finally a data multiplexer adds data from both Interface FIFOs to the data bus. The data bus is 28 Bits wide and capable of 40 MHz transfer rate. The data bus can be switched to 16 Bit width writing 0x0000010 into address 14. A LOW at pin 'Output enable' forces the bidirectional bus drivers to permanent output state. This is helpful for fast data read out routines.
Each Interface FIFO has an empty flag (EF) and a load-level flag (LF). All flags are HIGH active. At low data rates it is recommended to check the EF to see whether there are data available for read out. It is not allowed to read from an empty Interface FIFO. The LF is helpful at high data rates. The load level threshold can be set in 'Fill' in register 6 and is the same for both FIFOs. As soon as the set number of data is available this can be read from the FIFO as a block without the need of checking the EF.

Note: the load-level flags are not synchronized. The load-level flag for a FIFO is valid only if it is **not** read from this FIFO. Otherwise there might be spikes.

Quiet Mode
In M-Mode it is mandatory to use the Quiet mode.
In Quiet Mode the post-processing and calculation does not start automatically after each single event, but after a dedicated trigger. The trigger can be given externally by a rising slope at pin ALUTRIGGER or by software setting a dedicated ALU-Trigger Bit.
The time needed from the start of the post-processing until first data is available in the interface FIFO is typ. 900 ns.

5.4 Data structure and readout

The output results are integers with a LSB width defined by the setting of the resolution adjust unit, divided by MSet.

$$BIN = \frac{T_{ref} \times 2^{refclkdiv}}{216 \times hsdiv} \times \frac{1}{3} \times \frac{1}{MSet + 1}$$

Bit 27 … 23	Bit 22…0
Not used	Edge-to-Start result of the addressed combined channel

The data can be read from address 8 for interface FIFO1 and from address 9 for interface FIFO2.

5.5 Reset

There are 3 ways of resetting the device:

- **Power-up reset**: a low signal at pin PURESN resets the whole chip.
- **Master-Reset**: this command resets everything except the configuration registers. It can be done by software writing to register 4. In non-quiet mode MasterAluTrig in register 5 can be set to '1'. Then this command can be done also by a HIGH at the Alutrigger input pin. In quiet mode MasterOenTrig in register 5 can be set to '1'. Then this command can be done also by a LOW at the OEN input pin (only with OEN off).
- **Partial-Reset**: this command resets everything except the configuration registers and the Interface FIFOs. It can be done by software writing to register 4. In non-quiet mode Partial-AluTrig in register 5 can be set to '1'. Then this command can be done also by a HIGH at the Alutrigger input pin. In quiet mode PartialOenTrig in register 5 can be set to '1'. Then this command can be done also by a LOW at the OEN input pin (only with OEN off).

After a Power-on reset or a Master reset it takes 40 ns before the Start and Stop inputs accept data.
After a Partial reset it takes 75 ns before the Start and Stop inputs accept data.

5.6 MTimer

There is an internal timer available for internal use. The main application will be setting a dedicated time interval between 25ns and 204.7 µs after which the interrupt flag is set. The period is set in 'MTimer', register 7, in multiples of Tref. The maximum delay is 8191 * Tref = 204.7 µs. The timer can be started by a Stop and/or Start signal. This is set in 'MTimerStart' and 'MTimerStop', register 4. Setting Bit 'TimerFlag', register 12, the interrupt flag is set when the timer stops.

5.7 Interrupt Flag

The user can select on which event(s) the interrupt flag is set.
The selection is done in register 12, Bits 13 to 25, by unmasking the dedicated bits. They are combined by an Or-Gate to the interrupt flag.
Selectable events are

- Hit FIFOs 1, 2 ...or/and 8 are full
- Interface FIFOs 1 or/and 2 are full
- PLL not locked
- All Hit FIFOs empty
- End of Mtimer

5.8 Error Flag

The user can select on which event(s) the error flag is set.
The selection is done in register 11, Bits 16 to 26, by unmasking the dedicated bits. They are combined by an Or-Gate to the error flag.
Selectable events are

- Hit FIFOs 1, 2 ...or/and 8 are full
- Interface FIFOs 1, 2 ...or/and 8 are full
- PLL not locked

5.9 Testinputs

For test purpose a set of three TTL inputs can be multiplexed to the measuring circuit by setting Bit Gtest in register 3. The test inputs have the same functionality as the measure inputs, but can only handle a minimum pulse width of 5ns and a minimum edge-to-edge distance of 20ns.

5.10 M-Mode Timing & Resolution

TDC-GPX is working in resolution adjust mode.
The intrinsic delay parameters vary with voltage, temperature and process tolerance. The resolution adjust unit uses the voltage depency to compensate for temperature and process variations. The following table lists the derating factors.

Derating by	Minimal	Maximal
Voltage	0.91 at 3.6V	1.2 at 2.85V
Temperature	0.889 at –40°C	1.17 at +125°C
Process	0.74	1.31

With the stabilization of the resolution by the resolution adjust mode, the voltage of the core decreases with decreasing temperature, and increases with increasing temperature. The setting should be done in a way that at maximum operating temperature the maximum core voltage is reached, and that minimum core voltage is reached at minimum operating temperature. With this method you get two limits:

Best case process, deepest temperature, lowest voltage: 0.74 x 0.889 x 1.2 = 0.789
Worst case process, highest temperature, highest voltage: 1.31 x 1.17 x 0.91 = 1.394

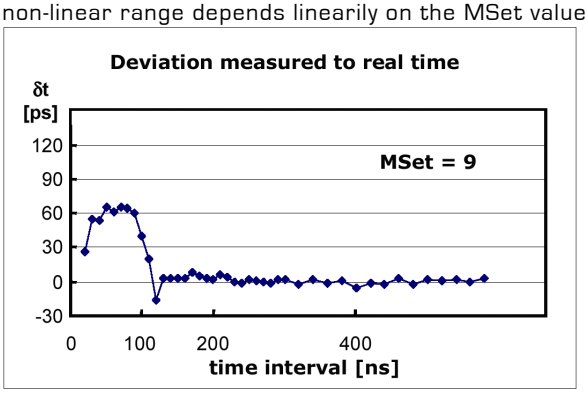
The BIN size is calculated as $BIN_{R\text{-}Mode}$/MSet. The standard deviation in M-Mode is basically limited by the noise of the measuring unit and has been measured with 10 ps + 8 ps * Δt/µs.. The BIN size has no real influence on this.

The pulse width limit is minimum 1.5 ns, limited by the input buffers.

The measurement range depends on the M-Mode bin size and the coarse counter. Its typical value is:

$$\text{Range} = 2^{23} \times BIN_{R-Mode} \times \frac{1}{MSet+1} \approx 7\mu s(MSet = 31)$$

INL
As a speciality of M-Mode the integral non-linearity shows a deviation of the measured to the real time interval in the near range. The width and height of the non-linear range depends linearily on the MSet value.



5.11 Measurement Flow

In the following we shows a typical example of register settings and measurement flow in M-Mode.

Task: Typical application laserscanner.
Given a Start signal with 10 kHz rate. To each Start there is one Stop event on channel 1. The time between Stop and Start shall be measured with high resolution, using the LVPECL inputs.
Choice: M-Mode, triggering the external laser,

```
//****** M-Mode, Stop against Start **********

PuResN=Low;                         // Power-up reset
PuResN=High;

StopDis1 = High;                    // Disable inputs
StopDis2 = High;
StopDis3 = High;
StopDis4 = High;
                                    // write configuration registers:
_oupd( 0,0x000008B);                // Rising edges, Start ringoscil.
_oupd( 1,0x0620620);                // Channel adjust = 6 & 2
_oupd( 2,0x0062004);                // R-Mode, channel adjust = 6 & 2
_oupd( 3,0x000001E);                // Use LVPECL inputs, MSet = 30
_oupd( 4,0x6000300);                // EFlagHiZN, Quiet Mode, M-Mode
_oupd( 5,0x0000000);                // -
_oupd( 6,0x8000000);                // Switch on ECL power
_oupd( 7,0x0001FB4);                // Bin = 0.8850ps (resolution ~ 10ps rms)
_oupd(11,0x7FF0000);                // Any error -> ErrFlag
_oupd(12,0x2000000);                // MTimer to IrFlag
_oupd(14,0x0000000);

_oupd( 4,0x2400001);                // Master reset

StopDis1 = Low;                     // Enable inputs
StopDis2 = Low;
StopDis3 = Low;
StopDis4 = Low;

do
{
   TriggerLaser;                          // send trigger to the laser

   while(!(_inpw(8) & 0x0020));           // Check Interrupt flag
   _outpd(4,0x7000300);                   // Reg4, ALU trigger
   while((_inpd(8) & 0x0800)>0);          // Check Empty flag

   FIFO0 = _inpd(8) & 0x7FFFFF;                          // Read FIFO0
   printf("%5.3fns\n",float(FIFO1)*27.4348/1000/31);  // Display time in ns

   _outpd(4,0x6400300);                   // Master reset
} while(!quit)
```

6 Bug Report

6.1 Data Bus: 16 Bit Mode

Subject:
CSN in 16-Bit mode
When working with a 16 Bit databus, register 14 Bit 4 = 1, there is a malfunction of CSN.

Relevance:
Systems with not only a TDC-GPX at the 16 Bit bus but other chips o TDCs connected too.

Description:
In 16 Bit mode we have two internal latches that collect the data for the high-word and the low-word and put them together to one 28 bit value. Strobes on RDN or WRN toggle between the two latches. This should be deactived when CSN is high but it is not.

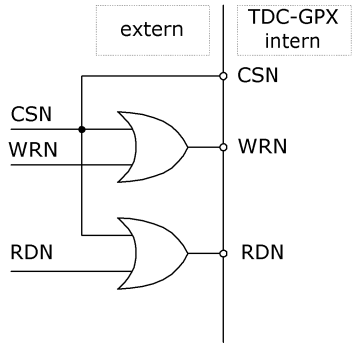
As long as CSN is high no data are written in the TDC-GPX but the latches are toggled. If CSN goes low and the pointer is already on the high-word latch then the data with the next RDN/WRN strobe will be wrong.

Workaround:

1. By Software
The following sequence at the beginning of any communication with the TDC-GPX will guarantee that the pointer shows to the low-word latch:

Write Adr = 15, Val = 0x00 (empty address)
Write Adr = 14, Val = 0x00
Write Adr = 14, Val = 0x00 now the 16 Bit mode is definitely off, latch pointers are correct
Write Adr = 14, Val = 0x10 Switch on 16 Bit mode again

2. By Hardware
Disable the RDN/WRN lines with CSN = High



7 Last Changes

8th Nov 2005	Additional comments, small corrections
16th Feb 2006	New TFBGA120 package
12th April 2006	Correction in sections 3.5, 4.5, 5.5.
31st May 2006	New section 1.6.3.

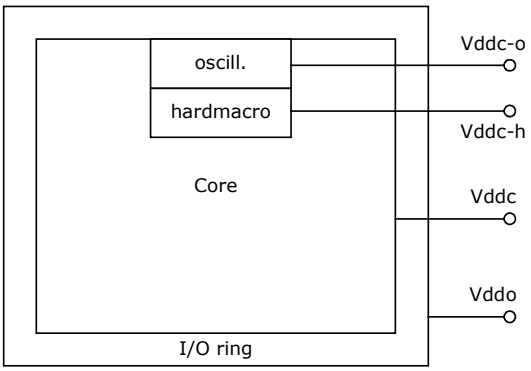
Contact

Headquarter Germany:	acam-messelectronic gmbh	Am Hasenbiel 27 D - 76297 Stutensee-Blankenloch	Tel: +49-7244-7419-0 Fax: +49-7244-7419-29 email: support@acam.de www.acam.de
Distributors :			
France	microel (CATS S.A.)	Immeuble "Oslo" - Les Fjords 19, avenue de Norvège Z.A. de Courtaboeuf - BP 3 91941 LES ULIS Cedex	Tél. : +33 1 69 07 08 24 Fax : +33 1 69 07 17 23 commercial@microel.fr www.microel.fr
India	Brilliant Electro-Sys. Pvt. Ltd.	4, Chiplunkar Building, 4 Tara Temple Lane, Lamington Road, Mumbai – 400 007	Tel: +91 22 2387 5565 Fax: +91 22 2388 7063 www.brilliantelectronics.com besimpex@vsnl.net
Israel	ArazimLtd.	4 Hamelacha St. Lod P.O.Box 4011 Lod 71110	Tel: 972-8-9230555 Fax: 972-8-9230044 email: info@arazim.com www.arazim.co.il
Italy	ESCO ITALIANA S.p.A.	Via G.B. Stucchi, 66/28 20052 Monza (MI)	Tel. : (+39) 039/20481 Fax : (+39) 039/2048234 email : milano@escoitaliana.it www.escoitaliana.it
Japan	DMD–Daiei Musen Denki Co., Ltd.	10-10, Sotokanda, 3-Chome, Chiyoda-Ku Tokyo 101-0021	Tel: +81 (0)3 3255 0931 Fax: +81 (0)3 3255 9869 www.daiei-dmd.co.jp sales@daiei-dmd.co.jp
P.R. China	Broadtechs Technology Co. Ltd.	Shanghai Office: 14C JinHuan Building, 489 Xiang Yang Road South Shanghai, 200031	Tel.: +86-21-54654391 Fax: +86-21-64454370 http://www.acam-china.com/ Email: info@acam-china.com
South Korea	SamHwa Technology Co., Ltd.	303-3 Hanlim Human Tower, #1-40 Gumjeong-Dong, Gunpo-City,Kyuggi-Do	Tel: +82 31 479 2580 Fax: +82 31 479 2589 www.isamhwa.com minjoonho@isamhwa.com
Switzerland	Computer Controls AG	Neunbrunnenstr. 55 8050 Zürich	Tel.: +41-1-308 6666 Fax: +41-1-308 6655 email: roeschger@ccontrols.ch www.ccontrols.ch
United States of America	Transducers Direct, LCC	264 Center Street Miamiville, Ohio 45147	Tel: 513-583-9491 Fax: 513-583-9476 email: sales@acam-usa.com www.acam-usa.com

TDC-GPX – PLL Regulation Circuits

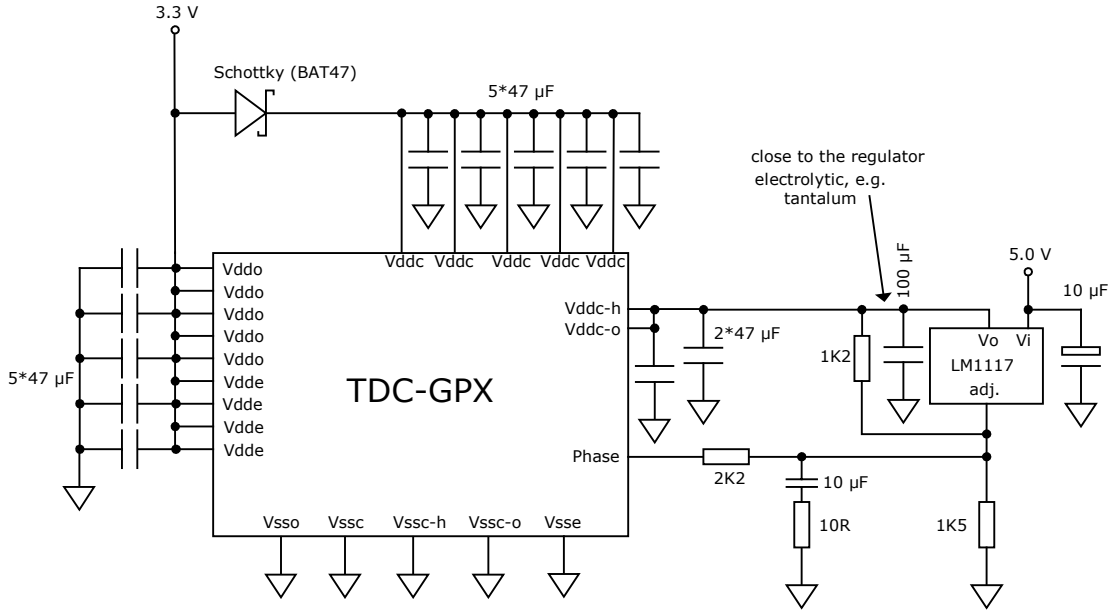
Introduction:
The TDC-GPX chip shows different blocks with separate power supplies:

Vddc-o,Vddc-h	Oscillator and Hardmacro This is the time interval measuring unit
Vddc	Core All digital circuitry besides the measuring unit (ALU, FIFO's etc.)
Vddo,Vdde	I/O Padring and LVPECL input buffers I/O buffers, input protection



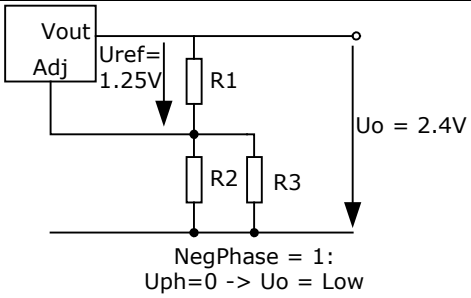
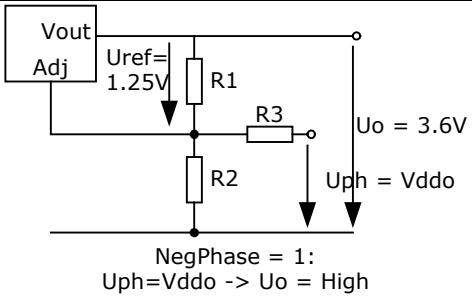
The purpose of the PLL regulation circuit is to keep the speed of the oscillator & hardmacro constant by regulating the voltage Vddc-o/h between 2.4 and 3.6V.

The recommended circuit is based on the LM1117. We strongly recommend to use only LM317 or LM1117 regulators. Only for these regulators the ciruit is tested and approved. Do not use low-drop regulators. This regulator's reference refers to the output voltage.

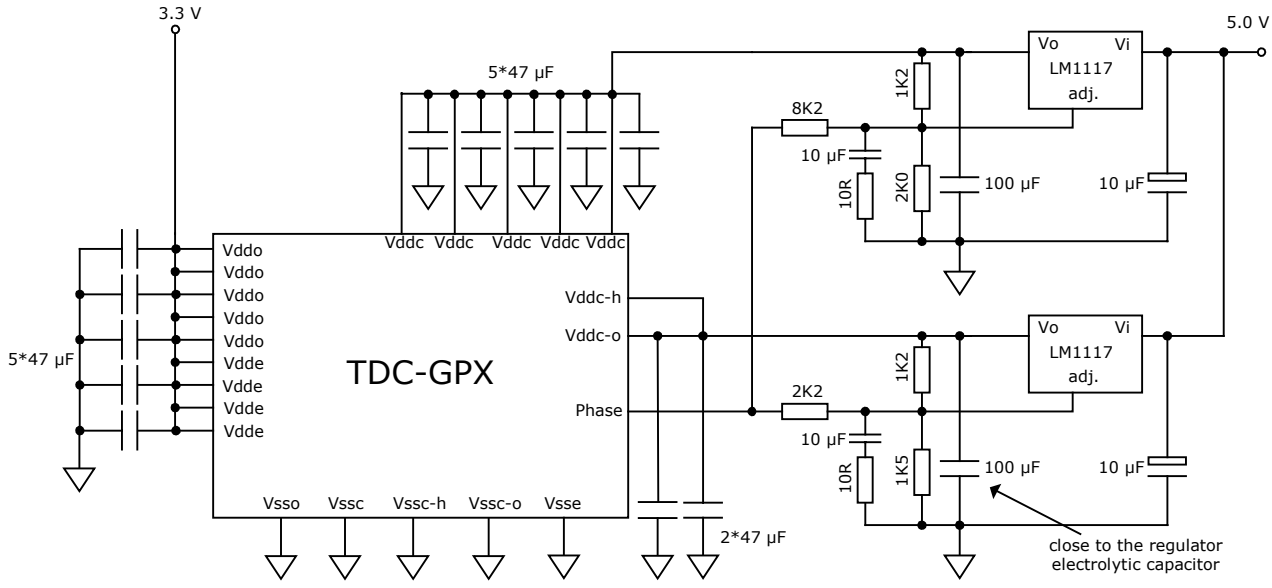


The IO buffers are supplied with 3.3V typically to be compatible with a 3.3V design. It is strongly recommended to use a linear regulator to provide the 3.3V. Switched mode regulators will introduce a lot of noise to the measurement. The core voltage is set to 3.0V. The easiest way to do this is to use a BAT47 schottky diode. The purpose is to avoid voltage differences bigger than 0.6V between Vddc and Vddo on the one side and Vddc and Vddc-o/h on the other.
The outputs' high-side switches do not fully close when Vddc is more than 0.6V below Vddo. Therefore other devices on the bus must be able to drive a few mA to pull the outputs down to LOW. This may be no problem for an FPGA and only one TDC-GPX connected to the bus. But of course this is a problem with weak drivers and more than one device on a bus.

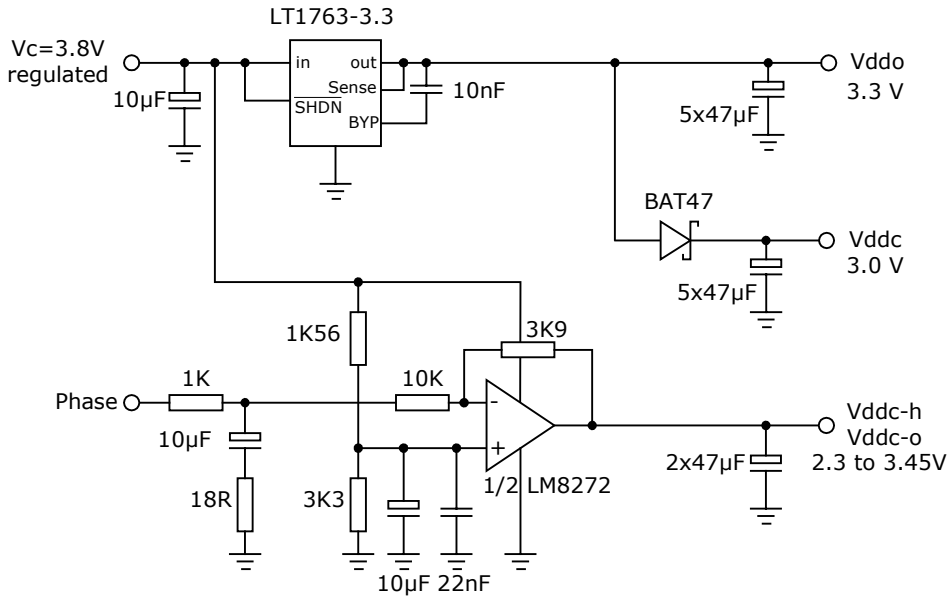
Calculating the resistors:
In the TDC-GPX application we look at two extremes:

1. Phase output has 0% duty cycle -> Low output voltage. In this case R2 and R3 are in parallel (R23).	2. Phase output has 100% duty cycle -> High output voltage. In this case R3 is at Vddo.
 NegPhase = 1: Uph=0 -> Uo = Low	 NegPhase = 1: Uph=Vddo -> Uo = High
For given resistor values the output levels are: $U_{min} = U_{ref} \times \left(1 + \frac{R_{23}}{R_1}\right) \qquad \frac{1}{R_{23}} = \frac{1}{R_2} + \frac{1}{R_3}$	$U_{max} = U_{ref} \times R_{23} \times \left(\frac{1}{R_1} + \frac{1}{R_{23}}\right) + U_{ddo} \times \frac{R_{23}}{R_3}$
For given vlotage levels the resistor are calculated like: $R_3 = \frac{U_{ddo}}{(U_{max} - U_{min})}\left(\frac{U_{min}}{U_{ref}} - 1\right) \times R_1 \qquad R_2 = \frac{U_{ddo}}{(U_{ddo} - U_{max} + U_{min})}\left(\frac{U_{min}}{U_{ref}} - 1\right) \times R_1$	

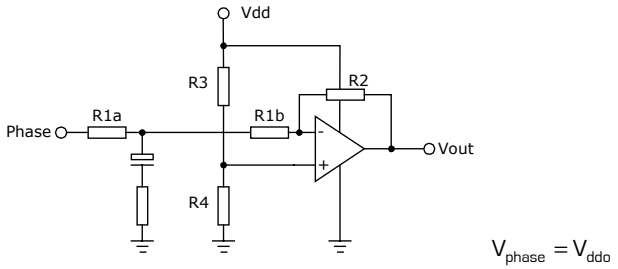
Extended regulation range:
The solution from above shows a slightly reduced regulation range. The reason is that the oscillator speed at Vddc-o/h = 3.6V & Vddc = 3.0V is a little bit less than with both voltages at 3.6V.
There is a solution to overcome this: using a second regulation circuit for Vddc instead of the schottky diode. The second regulator for Vddc has a regulation range from 3.0V to 3.6V. In other words: With TDC-GPX output phase=LOW regulator 1 delivers Vddc-o/h = 2.4V and regulator 2 delivers Vddc=3.0V. At phase=HIGH regulator 1 delivers Vddc-o/h = 3.6V and regulator 2 delivers Vddc=3.6V. Of course the circuit is alittle bit more complex.



Low-drop solutions:
The recommended circuit from above doesn't work with low-drop regulators. In applications where the power dissipation has to be as low as possible the following circuit can be used. In this circuit the voltage regulator is replaced by an operational amplifier.



The LM8272 has enough output power and is ecspecially designed to drive high capacitive loads.



$$U_{out} = U_{dd}\left(1+\frac{R_2}{R_1}\right)\frac{R_4}{R_3+R_4} - U_{phase}\frac{R_2}{R_1}$$

$$\frac{R_2}{R_1} = \frac{U_{max} - U_{min}}{U_{phase}}$$

$$\frac{R_3}{R_4} = \frac{U_{dd} \times \left(U_{phase} + U_{max} - U_{min}\right)}{U_{max} \times U_{phase}} - 1$$